The Dissertation Committee for Hsun-Cheng Lee
certifies that this is the approved version of the following dissertation:

Designs and Calibration of Delay-line Based ADCs

Committee:

Jacob A. Abraham, Supervisor

Ranjit Gharpurey

Michael Orshansky

Nan Sun

Chaoming Zhang

Designs and Calibration of Delay-line Based ADCs

by

Hsun-Cheng Lee, B.S.; M.S.

DISSERTATION

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

DOCTOR OF PHILOSOPHY

THE UNIVERSITY OF TEXAS AT AUSTIN

December 2015

Dedicated to my wife, Penny Shan-Kuei Pan
and my parents, Chin-Tu Lee & Chin-Yuan Lee.

Acknowledgments

First of all, I would like to show my sincere appreciation to my supervisor, Dr. Jacob A. Abraham. During the studies, He always encouraged me and helped me to do research. Without his guidance, support, and mentoring of my research, I would not have been able to complete this degree.

I would also like to thank Dr. Ranjit Gharpurey, Dr. Michael Orshansky, Dr. Nan Sun and Dr. Chaoming Zhang for serving as my dissertation committee members and providing useful advice. I would like to specially thank Professor Nan Sun for the insightful technical discussions and suggestions.

I would like to thank the laboratory members of Computer Engineering Research Center, Ameya Chaudhari, Ricardo Ramirez, Mahesh Prabhu, Shahrzad Mirkhani, Eun Jung Jang, Balavinayagam Samynathan, Li-Da Huang and Ce Wei for the help of resolving technical issues and questions. In addition, I would like to thank my friends at The University of Texas at Austin, Yi-Ting Chen, Leu-Ren Chen, Ming-Jun Chen, Chih-Hung Chen, Tony Che-Chuan Wu, Chia-Sheng Tsai, Wan-Shan Wu, Ginger Chen, Chao-Yeh Chen, and Anton Wei-Chen Wu.

I would like to thank the team members, Hazem Zawaideh, Abdigani Hussein, Craig Johnson, Bernd Kastenmeier, Francois-Xavier, and Donald Smelzer at Freescale Austin, where I had a great internship to learn and develop a novel electro-migration methodology. I would like to special thank the team manager, Ertugrul Demircan, who taught me a lot of technical knowl-

edge and resolved my questions. I would also thank the people in Intel Austin where I had my first internship in 2009, David Wu, Mark Lin, Wei Li and other team members. I was glad to have a chance to co-work with all of them.

Most importantly, I am grateful to my parents, Chin-Tu Lee & Chin-Yuan Lee, my brother, Yung-Feng Lee, my sisters, Mei-Fen Lee & Mei-Wen Lee for their endless support and sacrifice. Especially, I am very thankful to my wife, Penny Shan-Kuei Pan, and our son, Benjamin Yu-Che Lee. Without their support and sacrifice, I would never have been able to finish my degree.

Hsun-Cheng Lee
December 2015, Austin, TX

Designs and Calibration of Delay-line Based ADCs

Hsun-Cheng Lee, Ph.D.
The University of Texas at Austin, 2015

Supervisor: Jacob A. Abraham

Delay line ADCs become more and more attractive with technology scaling to smaller dimensions with lower voltages. Time domain resolution can be increased by high speed delay cells. A GHz sampling rate can be easily achieved with low power. However, linearity, which has always been an issue, becomes a problem with longer delay lines. Resolutions of reported delay-line ADCs are hardly more than 4 bits with sampling rates of hundreds of MHz. Thus, this dissertation addresses the linearity issue of delay line ADCs.

First, a novel 11-bit hybrid ADC using flash and delay line architectures, where a 4-bit flash ADC is followed by a 7-bit delay-line ADC, is proposed. In this structure, the noise/error of the second stage delay-line ADC is attenuated at the hybrid ADC output, such that the overall performance would not be limited by the poor linearity of the delay-line ADC. The achieved figure of merit (FOM) of 33.8 fJ/conversion-step is competitive with state-of-the-art ADCs. Furthermore, the proposed ADC inherits accuracy and high speed from the flash ADC and the delay-line ADC, respectively. The inherited advantages strongly support the scalability of the proposed ADC to provide a

better performance with low power in further scaled fabrication processes.

Second, in order to remove the harmonic distortion of delay-line ADC, we present a technique which extends harmonic distortion correction (HDC) to digitally calibrate a delay-line ADC. In our simulation results, digital calibration improves SNDR from 25.6 dB to 42.5 dB by averaging 2^{27} sample points, which corresponds to a 0.86 second calibration time.

Last, a multiple-pass delay line ADC is proposed to improve overall ADC performance in terms of speed and resolution. In this structure, a multiple-pass delay cell can be early triggered by the previous cell to increase speed. Also, phase interpolation is used to improve the effective number of bits. The design is designed and simulated in a commercial 40nm process technology. With 500MHz sampling rate, the multiple-pass delay line ADC achieves an SNDR of 37 dB and consumes 4.2 mW, which is competitive with other reported ADCs.

Table of Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Overview

Analog-to-digital converters (ADCs) are widely used in many applications, such as high-definition video systems, mobile communication devices, and local/wide area network equipment. High-resolution, high-speed and low power analog-to-digital converters are required to meet stringent demands for resolution, speed, and power-efficiency.

However, with the continued improvement of integrated circuit fabrication technology, the nanoscale regime comes with various complex effects which impede analog circuit scaling [16, 24]. In particular, the finite intrinsic gain of transistors makes designing an analog circuit more challenging. In current commercial sub-65nm processes, the intrinsic gain is less than 20, making amplifiers with gains of thousands difficult to design. In order to derive a high gain amplifier, many sophisticated architectures with gain boosting, and multiple stages are needed. However, this greatly increases the complexity of designs, and the stability is also a concern. In addition, voltage scaling results in noisier signals. Meanwhile, the relatively high threshold voltage greatly reduces the available signal headroom in any sophisticated analog design. Therefore, a new architecture or a new methodology is needed to eliminate the limitations in the nanoscale era.

Furthermore, voltage-based ADCs, which includes flash, pipeline and

successive approximation (SAR) ADCs have been widely studied for various applications [2, 3, 5, 10, 25, 26, 42, 43, 47]. However, with advances in process technology, voltage-based ADCs cannot be scaled down in terms of power and speed as can digital circuits [40]. Flash ADCs usually use small feature sizes to reduce the power consumption with a higher sampling rate. However, small size devices have the mismatch issue among components due to process variations. In order to tackle the mismatch issue, several calibration techniques are introduced, but calibration techniques are usually complex and require a bigger area and power overhead. On the other hand, SAR ADCs need to utilize the time-interleaved technique to achieve a high sampling rate, where a calibration technique is needed to eliminate the mismatch among the parallel paths. Therefore, the voltage-based ADCs cannot be scaled as well as digital circuits when the process features shrink, although using smaller devices implies that a faster sampling rate can be easily achieved, and lowering supply voltage can reduce power consumption.

Time-domain analog-to-digital conversion techniques, which include the voltage-to-time-to-digital approach and the voltage-to-delay-to-digital approach, have recently become attractive, especially for nanoscale technologies [16, 24, 40]. The voltage-to-time-to-digital conversion utilizes a voltage-to-time converter and a time-to-digital converter (TDC) to digitize the input signal, shown in Figure 1.1(a). According to the structure of the TDC, different resolutions can be derived. Figures 1.1(b) and 1.1(c) show two types of TDC structure, basic and vernier. The time resolution of the basic structure is the buffer delay, D, while the time resolution of the vernier structure is the difference between the two delay cells, δ, which is much smaller than the buffer delay, D. On the other hand, the voltage-to-delay-to-digital scheme controls

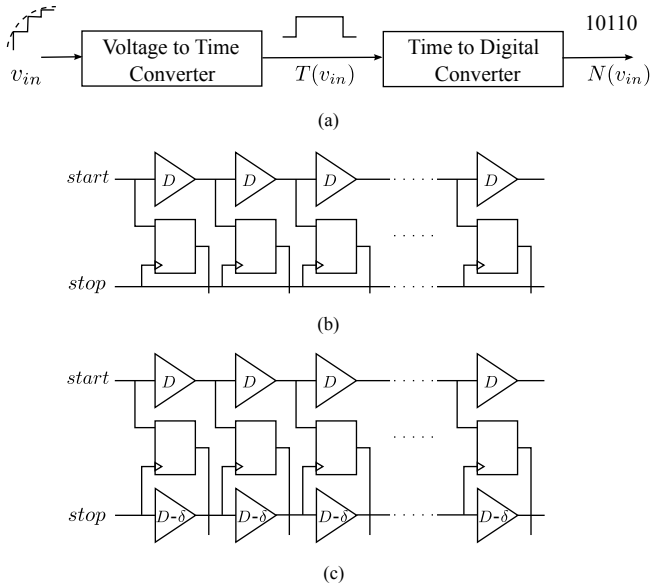

Figure 1.1: (a) The diagram of voltage-to-time-to-digital ADCs. (b) Basic structure of TDCs. (c) Vernier structure of TDCs.

the delay of buffers instead of the time window. Figure 1.2 shows a diagram of a voltage-to-delay-to-digital ADC, where the input voltage is digitized by the number of delay cells that the signal passes through in a fixed time window. Generally, time-domain ADCs receive advantages from advances in fabrication technology. A GHz sampling rate can be easily derived [24, 40]. However, non-linearity is still an issue, so that the resolution is hardly more than 4 bits with a hundred MHz sampling rate. Therefore, this dissertation addresses the linearity issue of delay-line ADCs.

1.2 Motivation and Goals

In order to overcome the design challenge of delay-line ADCs, this dissertation introduces a novel hybrid architecture and a multiple-pass delay line

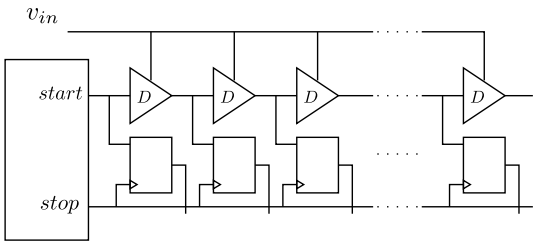

Figure 1.2: The diagram of voltage-to-delay-to-digital ADCs.

ADC; digital calibration techniques are also discussed. In this section, we will discuss our motivation and goals of the new architecture and calibration techniques.

1.2.1 New Architecture and Design

With the process technology improvements, voltage based ADCs, including flash ADC and SAR ADCs, cannot scale as well as digital circuits. Also, although time-domain ADCs benefit from advances in fabrication technology, non-linearity is still a big concern. Nonetheless, the linearity of voltage-based ADCs is very good, while time-domain ADCs can easily operate at a GHz sampling rate. Currently, several different architectures have been studied [27, 34, 43] to utilize the advantages of voltage based ADCs and time-domain ADCs. Mesgarani *et al.* proposed a 5-bit delay-based pipelined ADC in [27], which benefits from the high speed of delay cells. Verbruggen *et al.* presented a 11-bit interleaved pipelined SAR ADC [43], which exploits the high accuracy of SAR ADCs. Sanyal *et al.* designed a hybrid SAC-VCO $\Delta\Sigma$ ADC [34], which uses the advantages of the high speed of delay cells and the high accuracy of SAR ADCs. In this dissertation, we propose a novel low power 11-bit hybrid ADC architecture, where a 4-bit flash ADC is followed by a 7-bit delay-line ADC [22]. In this structure, the first-stage 4-bit flash ADC

first provides a very accurate result, while the second-stage 7-bit delay-line ADC quantizes the residue of the first stage ADC in 1.6 ns. Thus, this hybrid ADC can inherit accuracy and high speed from the flash ADC and the delay-line ADC, respectively, such that the overall performance would not be limited by the poor linearity of the delay-line ADC, since the noise of the second stage delay-line ADC is greatly attenuated at the ADC output.

Also, a multiple-pass delay line ADC with a phase interpolation technique is presented to further increase the speed and the resolution of delay-line ADCs such that the overall ADC performance can be improved. The multiple-pass structure has been used in the ring oscillator of a phase-lock loop (PLL). In this structure, multiple-pass delay cells are triggered early by the previous cells to increase speed. Also, phase interpolation is employed to generate extra phases from the outputs of neighboring delay cells with the same frequency such that the number of bits is increased. Therefore, the overall performance of the multiple-pass delay line ADCs with the phase interpolation technique can be improved in term of speed and resolution.

1.2.2 Digital Calibration Technique

With continued advances in integrated circuit fabrication technology, operation speed, area, and power have been significantly improved. Meanwhile, many accompanying complex effects impede analog circuit scaling [16, 21, 24]. Nonetheless, the increased density and speed of the transistors can, however, be exploited by using digital calibration to improve the precision of analog circuits. Figure 1.3 shows that the transistor counts in microprocessors increases exponentially over time [45]. Digital calibration is a technique to digitally estimate and cancel error/distortion and it has been widely used in

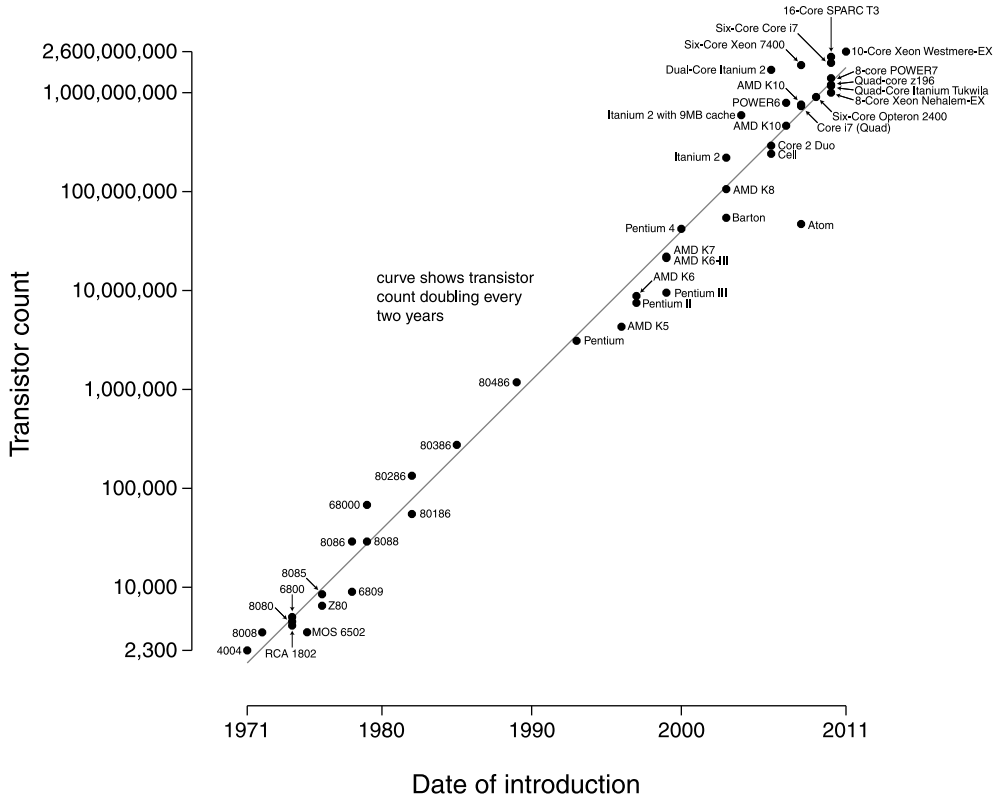

Figure 1.3: Microprocessor Transistor Counts 1971-2011 [45].

pipeline ADCs [9, 29, 30, 35]. Harmonic distortion correction (HDC) is one of the digital calibration techniques which can effectively remove the harmonic distortion of pipeline ADCs. In this dissertation, we extend harmonic distortion correction (HDC) to digitally calibrate a delay-line ADC [21] whose performance is limited by its harmonic distortion.

1.3 Organization of the Dissertation

In the dissertation, the novel hybrid ADC is introduced in Chapter 2. Chapter 3 presents our digital calibration techniques which extends HDC for

the calibration of a delay-line ADC. In Chapter 4, a multiple-pass delay-line ADC is described. Last, the conclusions and directions for future work are given in Chapter 5 and Chapter 6, respectively.

Chapter 2

A Novel 11-bit Hybrid ADC using Flash and Delay Line Architectures

2.1 Background

In order to improve the linearity of delay-line ADCs, a novel hybrid architecture is proposed in this Chapter. The proposed hybrid ADC uses a 2-stage pipeline structure where a 4-bit flash ADC is followed by a 7-bit delay line ADC.

The pipeline structure has been widely used in analog-to-digital conversion, especially for Nyquist sampling applications with high resolution and high speed [29, 30]. The resolution is in the range of 10 to 16 bits and the bandwidth is in the range of 15 to 250 MHz. Figure 2.1 shows an example of a pipeline ADC which contains 6 stages. In each stage, the input, $v_{in,k}$, is quantized to a 4-bit digital number, $x_k[n]$, and then a 4-bit DAC converts $x_k[n]$ to an analog signal. Finally, a residue amplifier amplifies the residue, v_k, by 8 and then sends the amplified residue to the next stage as input. After the following stages complete the conversion, the sum of $x_k[n]$ and the result of the next stage divided by 8 is sent to the previous stage. The noise in a previous stage can be attenuated by 1/8 in the current stage. As a result, the

The project is supervised by Jacob A. Abraham. [22] H.-C. Lee and J. A. Abraham, "A novel low power 11-bit hybrid ADC using flash and delay line architectures," Design, Automation and Test in Europe Conference and Exhibition (DATE), pp. $1-4$, 2014.

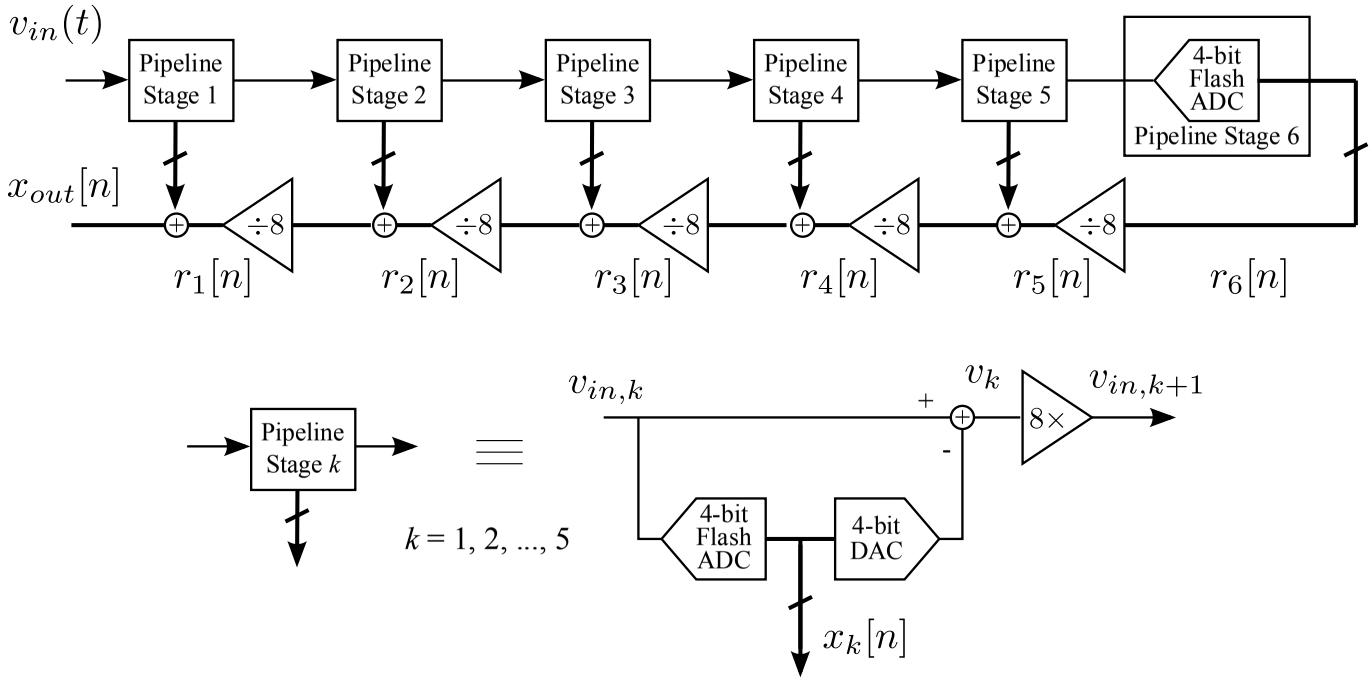

Figure 2.1: A 6-stage pipeline ADC.

noise of the last stage can be mitigated by $1/8^5$ at the output, $x_{out}[n]$.

Currently, many researchers have begun to study different architectures [27, 43]. Mesgarani *et al.* proposed a 1.25 Gs/s 5-bit delay-based pipelined ADC in [27], while Verbruggen *et al.* presented a 11-bit interleaved pipelined SAR ADC with power consumption of 1.7mW and 250 MS/s sampling rate. All of these also adopt the pipeline structure and attempt to benefit from advances in process technology. In this chapter, we propose a 11-bit hybrid ADC architecture, which is a 2-stage pipeline ADC where a 4-bit flash ADC is followed by a 7-bit delay line ADC. In this structure, the first-stage 4-bit flash ADC first provides a very accurate result, while the second-stage 7-bit delay-line ADC quantizes the residue of the first stage ADC with a sampling rate of hundreds of MHz. Intuitively, the error/noise in the second stage 7-bit delay line ADC is attenuated by 1/8 in the overall output. A detailed analysis is provided in Section 2.4. Therefore, the overall performance of the proposed ADC cannot be hurt by the poor linearity of the delay-line ADC. Furthermore, the proposed ADC inherits accuracy and power efficiency from the flash ADC and the delay-line ADC, respectively. These inherited advantages strongly support the scalability of the proposed ADC to provide better performance with low power in further scaled fabrication processes.

The remainder of this chapter is organized as follows. Section 2.2 introduces our hybrid ADC architecture. Section 2.3 presents the delay-line based ADC. Section 2.4 discusses the noise sources of the hybrid ADC. The proposed implementation is described in Section 2.5. Section 2.6 gives the simulation results. Finally, concluding remarks are made in Section 2.7.

2.2 Hybrid ADC architecture

Figure 2.2 shows the diagram of the hybrid ADC, where a 4-bit flash ADC is followed by a 7-bit delay-line ADC. In the first stage, the 4-bit flash ADC quantizes the input, v_{in} to a 4 bit digital result, x_1, and then the 4-bit digital-to-analog converter (DAC) converts x_1 to an analog signal, v_1, where $v_1 = x_1 = v_{in} + e_1$, and e_1 is the quantization noise of the 4-bit flash ADC. Let d_1 denote the digital output corresponding to x_1, where $d_1 \in \{0, 1, 2, ..., 15\}$. Then, $x_1 = d_1/16 \times V_{FS}$ where $V_{FS} = \max(v_{in}) - \min(v_{in})$. Next, between the first stage and the second stage, a subtracter, implemented by a switched-capacitor circuit, generates the residue of the flash ADC, $v_r = v_{in} - v_1$, and amplifies v_r by 8X. In the second stage, the 7-bit delay-line ADC receives the amplified residue, v'_{in} from the first stage flash ADC, and quantizes v'_{in} to x_2. Furthermore, x_2 is divided by 8. Finally, x_1 and $x'_2 = x_2/8$ are combined into the overall output of the hybrid ADC, x_{out}.

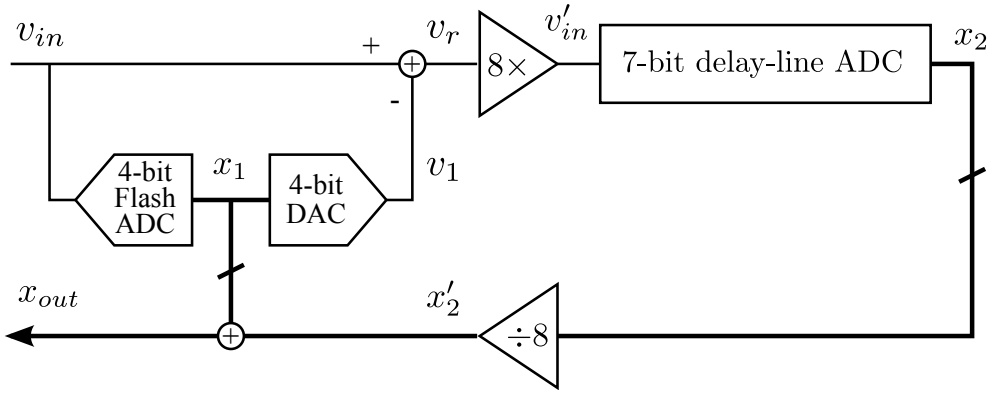

Figure 2.2: The hybrid ADC architecture.

Also, x_2 is the quantization result of the delay line ADC but not the

number of delay cells the signal passes though in a given time T, N_T. The relation between x_2 and N_T is $x_2 = \frac{N_T}{m+1} \times \frac{V_{\mathrm{FS}}}{2}$ where $m = N_T(\max(v_{in})) - N_T(\min(v_{in}))$ and $V_{\mathrm{FS}} = \max(v_{in}) - \min(v_{in})$. Thus, we can derive $x_{out} = x_1 + x_2/8 = \frac{d_1}{16} \times V_{\mathrm{FS}} + (\frac{N_T}{m+1} \times \frac{V_{\mathrm{FS}}}{2})/8$. For simplicity of implementation, the overall digital output, d_{out} is simplified to $(m+1)d_1 + N_T$. Note that $m = 41$ in the simulations that have been performed to evaluate the design.

2.3 Delay-line based ADC

In this section, we will discuss the second-stage delay-line ADC, which is a voltage-to-delay-to-digital ADC shown in Figure 1.2. The delay of the delay cells, $Delay(v_{in})$, is controlled by input signal, v_{in}. Thus, the number of delay cells, $N_T(v_{in})$, the signal passes through in a fixed time, T, can be written as $N_T(v_{in}) = \lfloor T/Delay(v_{in}) \rfloor$ where $\lfloor \bullet \rfloor$ denotes the floor function. In general, the delay of a delay cell, $Delay(v_{in})$, can be written as follows.

$$Delay(v_{in}) = \frac{C \cdot V_T}{I(v_{in})} + T_0 \tag{2.1}$$

where C is the capacitance at the charging node, V_T is the switching threshold voltage of the inverter, T_0 is the extra delay caused by the inversion and $I(v_{in})$ is the current controlled by v_{in} [33, 40, 44]. For short-channel MOSFETs in saturation mode, the drain current, I_d can be written as follows.

$$I_d = \frac{1}{2}\mu C_{ox}\frac{W}{L}\frac{(v_{gs} - v_{th})^2}{1 + \theta(v_{gs} - v_{th})}(1 + \lambda v_{ds}) \tag{2.2}$$

where θ is the parameter for the short-channel effects related to velocity saturation and mobility degradation due to the vertical field of the channel, and λ

is the parameter for the channel modulation due to the drain-source voltage, v_{ds}. From Equations 2.1 and 2.2, we know that $N_T(v_{in})$ is not linearly proportional to the input, v_{in}. Thus, $N_T(v_{in})$ can be rewritten in the following form.

$$N_T(v_{in}) = \lfloor a_0 + a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 + ... \rfloor$$

where a_i is the coefficient of the i-th term in the Taylor expansion of $N_T(v_{in})$. Since the quantization result of the delay line, x_2 equals $\frac{N_T}{m+1} \times V_{\mathrm{FS}}$, x_2 can be written as follows.

$$x_2(v_{in}) = b_0 + b_1 v_{in} + b_2 v_{in}^2 + b_3 v_{in}^3 + ... + e_2$$

where $b_i = \frac{a_i}{m+1} \times V_{\mathrm{FS}}$, and e_2 is the quantization noise of the delay line ADC. It shows that the delay line ADC introduces not only quantization noise, but also harmonic distortions.

Figure 2.3 is the spectrum of a 7-bit delay line ADC with a 312.5 MHz sampling rate and a 120 MHz sinusoidal wave input. (Note the period of a cycle = 3.2 ns, and the duty cycle = 50%, whose time window is the same as that of our second-stage delay-line ADC.) The SNDR is 28.7 dB, and the spurious free dynamic range (SFDR) is 29.0 dB. This confirms that delay line ADCs introduce not only quantization noise, but also harmonic distortion which limits greatly the SNDR of delay line ADCs.

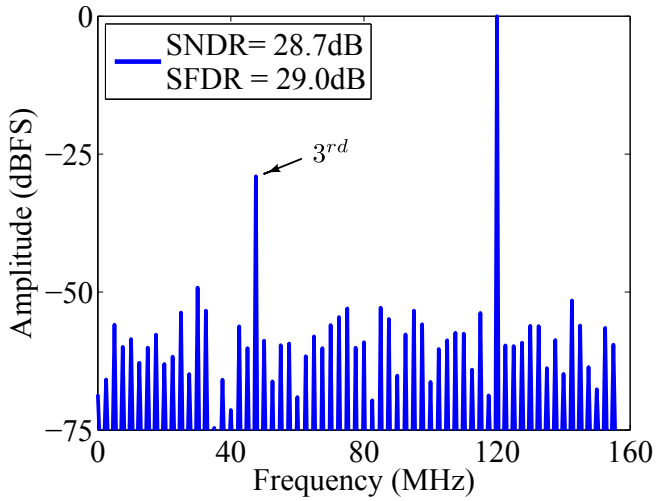

Figure 2.3: The spectrum of a 7 bit delay ADC.

2.4 Noise sources of the hybrid ADC

To demonstrate the noise sources of the hybrid ADC, we first consider the noise in the first stage flash ADC and then discuss the harmonic distortion introduced by the second stage delay-line ADC, since Figure 2.3 also shows that the third harmonic distortion of the delay line ADC limits the overall resolution, while the others are under the noise floor. The total noise of the hybrid ADC can be derived by combining these two contributions to noise.

2.4.1 Noise of the first stage flash ADC

With technology improvements, amplifers are becoming the dominating noise source in a switched-capacitor circuit implemented in deep-submicron CMOS technology. Therefore, a noise model is necessary to accurately consider all noise sources ultimately presented by the $\frac{kT}{C}$ noise.

For noise estimation of the first stage flash ADC, the Cline-Gary model with the parasitic loading effect is used [8, 11]. Figure 2.4 shows the singled circuit diagram of the hybrid ADC with all noise sources. The g_m block models the residue amplifier, while r_1, r_2 and r_3 represent the switch on-resistance. For generality, we discuss an n-bit flash ADC, and use the derived noise equation to calculate the noise of the first stage flash ADC. Thus, we know that $C_s = 2^n C_f$. Also, In this model, the loading from the amplifier, the comparators and the switches and the wiring are formulated by two capacitors, C_o at the output node and C_g at the summing node. In addition, C_L models the loading from the second stage delay-line ADC.

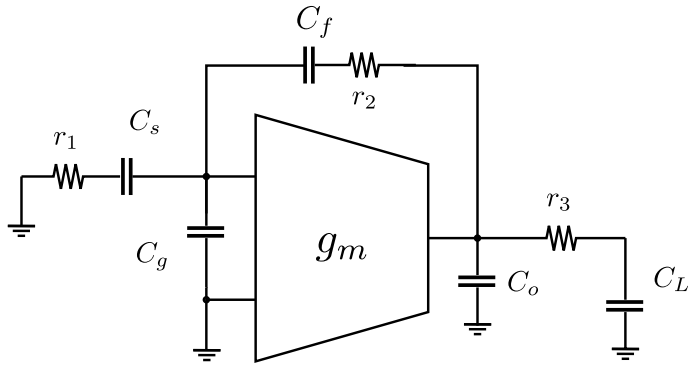

Figure 2.4: Noise model of the first ADC.

At the architectural level, considering the dependences between the conversion speed, the transcoductance of the amplifier, and the parastic-loading effects, C_g and C_o are defined by $C_g \approx C_o \approx \eta(2^n C_f)$, where η denotes a speed factor varying between 0 and 1 [8]. When the conversion speed is low, the parasitic loading is not severe and the load of the residue amplifier is dominated by the sampling capacitors. Thus, the speed factor, η, is small and can

be set to 0. When the conversion speed is high, the analysis is more technology dependent. The relationship between η and the sampling rate can be derived for a given technology. For the generality of analysis, the maximum parasitic capacitance is set to equal the total sampling capacitance, i.e., $C_o \approx C_g \approx 2^n C_f$ or $\eta = 1$. Thus, a feedforward factor, α, can be defined as

$$\alpha = \frac{C_s}{C_s + C_f + C_g} = \frac{1}{1 + 1/2^n + \eta} \tag{2.3}$$

and a feedback factor, β, can be derived as

$$\beta = \frac{C_f}{C_s + C_f + C_g} = \frac{1/2^n}{1 + 1/2^n + \eta}. \tag{2.4}$$

Considering a first-order frequency response, the g_m noise floor is defined by $\left(\frac{1}{\beta}\right)^2 4kT\frac{N_{op}}{g_m}$, where N_{op} is the noise factor of the amplifier. For long-channel devices, where the noise is mainly contributed by the input transistor, $N_{op} = 2/3$. For short-channel device, the noise factor, N_{op} is bigger than 2/3 and usually set to 3. In addition, the residue amplifier in the first stage ADC is implemented by a two stage folded-cascode amplifier, shown in Figure 2.10. Current sources biased by V_{b1}, V_{b4}, and V_{cmfb} in Figure 2.10 generate noise at the output as much as the input devices, and the input devices of the second stage also produce noise at the output. Thus, in this analysis, N_{op} is assumed to be 6.

In this analysis, instead of accurate second-order effects, we consider a first-order frequency response. In addition, the noise transfer function of the switches, r_1, r_2, and r_3, which are band-limited by the amplifier and determined by the low pass filter formed by the switch and the sampling capacitors,

can be calculated individually. Thus, the total noise floor of the first-stage ADC can be estimated as follows.

$$N_1(f) = 4kT \cdot \left[\left(\frac{1}{\beta}\right)^2 \frac{N_{op}}{g_m} + \left(\frac{\alpha}{\beta}\right)^2 r_1 + r_2 + r_3 \right] \tag{2.5}$$

where the first term is the amplifier noise, and the rest are the switches noise. Also, considering the settling speed of the switches with the settling speed of the amplifier, we assume

$$r_1 C_s, r_2 C_f, r_3 C_L \leq \frac{1}{5} \frac{1}{\omega_{-3dB}} = \frac{1}{5} \frac{C_c}{\beta g_m} \tag{2.6}$$

where C_c is the compensation capacitance of the residue amplifier.

Combining 2.5 and 2.6, we can derive

$$N_1(f) = \frac{4kT}{5g_m} \cdot \left[\frac{5N_{op}}{\beta^2} + \left(\frac{\alpha}{\beta}\right)^2 \frac{C_c}{\beta C_s} + \frac{C_c}{\beta C_f} + \frac{C_c}{\beta C_L} \right]. \tag{2.7}$$

The input-referred integrated noise is

$$N_1 = \frac{1}{4^n} \left[\frac{\pi}{2} N_1(f) BW \right] = \frac{1}{4^n} \frac{kT}{5C_f} \cdot \left[\frac{5N_{op}}{\beta C_c / Cf} + 2^n + 1 + C_f / C_L \right] \tag{2.8}$$

where BW denotes the bandwidth of the amplifier.

2.4.2 Noise and distortion of the second stage delay-line ADC

To demonstrate the noise and distortion of the delay-line ADC, we only consider the third harmonic distortion introduced by the second stage delay-line ADC, since Figure 2.3 also shows that the third harmonic distortion of

the delay line ADC limits the overall resolution, while the others are under the noise floor. In this section, the first flash ADC is assumed ideal, since the noise of the flash ADC, discussed in Section 2.4.1, can be added afterwards. Thus, the quantization result of the delay line ADC, x_2 can be simplified as follows.

$$x_2(v_{in}) = v_{in} + b_3 v_{in}^3 + e_2$$

Note that the even terms of harmonic distortions can be easily canceled in a differential circuit. In Figure 2.2, we know that the input of the delay-line ADC, $v'_{in} = 8e_1$. Thus, the quantization result, x_2 can be written as follows.

$$x_2(v'_{in}) = 8e_1 + 8^3 b_3 e_1^3 + e_2$$

Then, the overall output, x_{out} can be derived as follows.

$$\begin{aligned} x_{out}(v_{in}) &= v_{in} + 8^2 b_3 e_1^3 + e_2/8. \\ &= v_{in} + 4 \times 8^2 \times \text{HD3} \times e_1^3 + e_2/8 \end{aligned}$$

where $\text{HD3} = \frac{1}{4} \times \frac{b_3}{b_1} = -29$ dB.

Let NS_1 and NS_2 denote the terms from the harmonic distortion and the quantization noise of the second-stage ADC, repectively, i.e. $NS_1 = 4 \times 8^2 \times \text{HD3} \times e_1^3$ and $NS_2 = e_2/8$. We assume that the distributions of the quantization noises of two ADCs are uniform. The power of NS_1 and NS_2, P_{NS_1} and P_{NS_2} can be derived as follows.

$$P_{NS_1} \approx 256^2 \times \mathrm{HD3}^2 \times \frac{1}{7}(\frac{V_{FS}/16}{2})^6 \quad (2.9)$$

$$P_{NS_2} \approx \frac{1}{64}\frac{1}{12}(\frac{\frac{V_{FS}}{2}/42}{2})^2 \quad (2.10)$$

From Equations 2.9 and 2.10, we know that P_{NS_2} is much bigger than P_{NS_1}. That implies that the quantization noise of the second-stage delay-line ADC dominates the noise introduced by the harmonic distortion of the delay-line ADC in the proposed hybrid ADC.

Also, the jitter noise analysis is important for a delay line. Jitter has been widely studied in the design of ring oscillators [1, 15]. In each delay cell, the jitter components are independent of each other, and the variance of the jitter in time T is $\sigma_T^2 = \kappa^2 T$ where κ is a proportionality constant determined by circuit parameters [15]. Thus, jitter accumulates linearly with N_T, the number of delay cells the signal passes through in time T. For a delay cell with delay D, the equivalent input voltage noise power corresponding to σ_T^2 is $\mathrm{LSB}^2 \cdot \sigma_T^2/D^2$ [24]. In our delay cell design, $D \approx 28$ ps, and from simulation results, we obtain $\sigma_T = 3.54$ ps. The jitter equivalent input noise power is $0.015 \cdot \mathrm{LSB}^2$, which is significantly smaller than quantization noise and can be ignored.

2.4.3 Total noise of the hybrid ADC

We derive the total input-referred integrated noise of the hybrid ADC as follows.

$$
\begin{aligned}
N_{\text{hybrid}} &= \frac{kT}{C_s} + N_1 + N_2 \\
&= \frac{kT}{C_s} + \frac{1}{4^n}\frac{kT}{5C_f} \cdot \left[\frac{5N_{op}}{\beta C_c/Cf} + 2^n + 1 + C_f/C_L\right] \\
&+ 256^2 \times \text{HD3}^2 \times \frac{1}{7}(\frac{V_{FS}/16}{2})^6 + \frac{1}{64}\frac{1}{12}(\frac{\frac{V_{FS}}{2}/42}{2})^2 \qquad (2.11)
\end{aligned}
$$

where $\frac{kT}{C_s}$ denotes the noise of the front-end S/H circuit and N_2 denotes the noise from the second stage delay-line ADC. In our hybrid ADC, $n = 3$, $C_s = 300fF$, $C_c = 50fF$, and $C_L \approx C_s$. Thus, in the situation of temperature $T = 300K$ and the speed factor $\eta = 1$, we can derive SNDR $\approx$ 52.9 dB and ENOB $\approx$ 8.5 bits. For the differential input, the estimated SNDR $\approx$ 55.9 dB and the esitmated ENOB $\approx$ 9.0 bits.

2.5 Proposed Implementation

The fundamental building blocks of the hybrid ADC are a sample and hold (S/H) circuit, a 4-bit flash ADC, a 4-bit DAC, a subtracter, and a delay line ADC, which will be described in the next subsections.

Figure 2.5 illustrates the timing diagram of the hybrid ADC. There are three timing phases, ϕ_1, ϕ_2, and ϕ_3 and Figure 2.6 shows a phase generation for ϕ_1, ϕ_2, and ϕ_3, where ϕ is a reference clock. First, the S/H circuit samples the input signal in ϕ_1, and then the Flash ADC starts to quantize and the DAC converts the quantized result to an analog signal in ϕ_2. In ϕ_3, the subtracter generates the amplified residue of the first stage, and meanwhile the S/H circuit of the second stage holds the result. In ϕ_1 of the next cycle, the second stage delay-line ADC generates the fine result, while the S/H circuit of the first stage is sampling the next input.

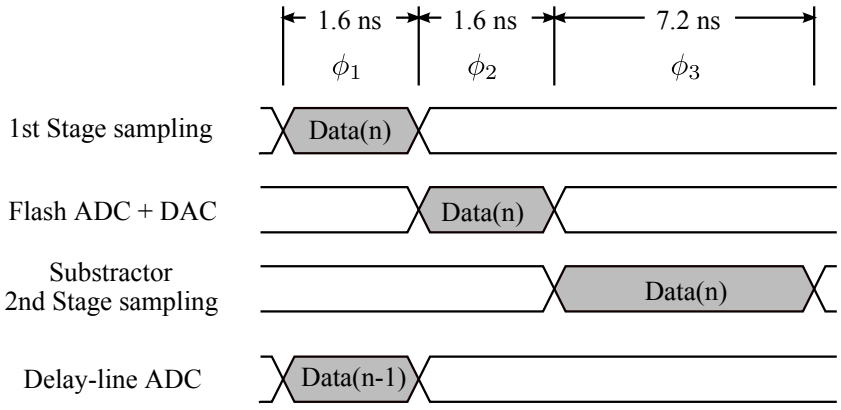

Figure 2.5: Proposed timing diagram for the hybrid ADC.

2.5.1 S/H circuit

Figure 2.7 shows the diagram of the bootstrapped switch [2, 25]. At the very beginning of each conversion cycle, the bootstrapped switch tracks the input signal and then holds the signal value when the bootstrapped switch is off. During tracking, the bootstrapped capacitor can ensure the gate-source voltage of the sampling transistor is at the supply voltage (V_{DD}). That maintains the on-resistance of the switch at a small value, so that the switch linearity is improved.

2.5.2 4-bit Flash ADC and 4-bit DAC

The first stage of the hybrid ADC uses a 4-bit flash ADC to digitize the input and then converts the digital result to an analog signal by a 4-bit DAC. The 4-bit flash ADC is composed of 15 comparators, and each comparator compares the input with a reference voltage. Figure 2.8 shows the diagram of the comparator. First, the input signal is pre-amplified and then the re-

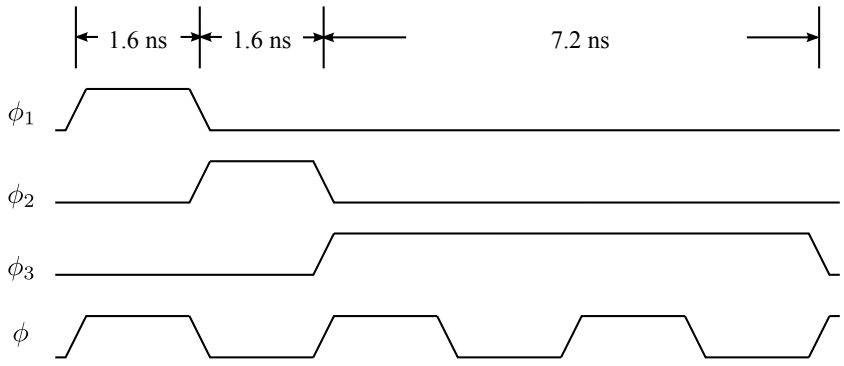

Figure 2.6: Phases generation for ϕ_1, ϕ_2, and ϕ_3.

generative latch compares the two inputs. Finally, the result is stored in the D-latch. The gain of the pre-amplifier is ∼20 dB, which can lower the input referred offset of the latch and attenuate kickback noise from the latch. The DC tail current of the pre-amplifier is biased at 47 μA. In order to reduce the power of the pre-amplifier, the bias voltage, V_{bias} is set to 250 mV after the regenerative latch operates, which can significantly reduce the tail current to 5 μA. To ensure the pre-amplifier works properly, V_{bias} is restored to a normal voltage at the time of 3.1 ns before the latch starts to work. Note that V_{bias} when the latch does not operate is set to 250 mV rather than 0 mV, since the restoration time of V_{bias} from 0 mV to the normal voltage is much longer and the tail current has been greatly reduced when being biased to 250 mV.

Also, when Clk is high, the regenerative latch compares the two outputs from the pre-amplifier and forces one output to high and the other to low according to the comparison result. When Clk is low, the D-latch stores the result, and meanwhile, the outputs of the regenerative latch are reset to high. After the 4-bit flash ADC generates the thermometer code, T<15:1>, the 4

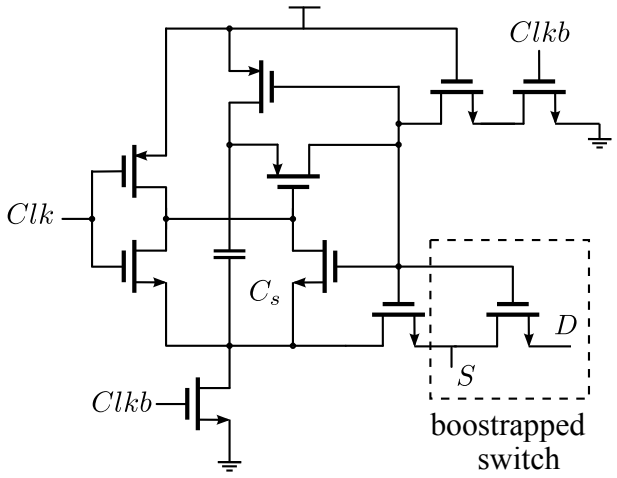

Figure 2.7: Bootstrapped switch.

bit DAC converts T<15:1> to a corresponding analog value according to two neighboring bits, shown in the left-hand side of Figure 2.9, and the analog signal is fed to the subtracter as an input, shown in the right-hand side of Figure 2.9.

2.5.3 Subtracter

The right-hand side of Figure 2.9 shows the subtracter, which is a switched-capacitor circuit, and whose inputs are the sampled signals of input, v_{in} and the DAC result. At the beginning of the conversion, ϕ_1, the subtracter samples v_{in}, and then at ϕ_3, the subtracter amplifies the difference of v_{in} and the DAC output by 8X, and connects the output to the second stage. Note that $C_s/C_f = 8$.

Figure 2.10 shows the operational amplifier (OPAMP), which is a two-stage folded cascode amplifier, used in the subtracter. The input and output

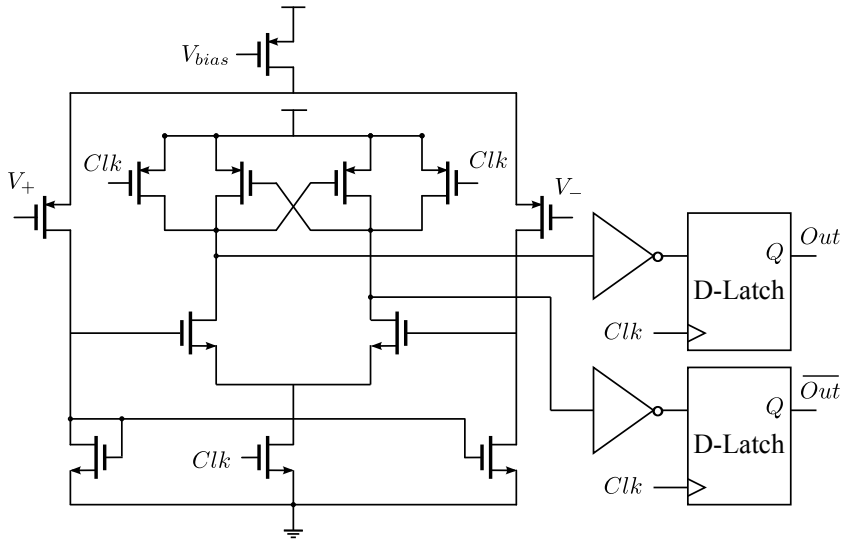

Figure 2.8: The schematic of the comparator.

common-mode voltages are designed to be 0.55 V, and the differential inputs of OPAMP is PMOS, while the inputs of the second stage is NMOS, since the transition frequency of NMOS is higher, which allows the second pole of OPAMP to be further from the first pole to improve the stability of OPAMP. Also, a Miller-compensation capacitor is used to improve the stability of the OPAMP. From the simulation results, the DC gain is around 60 dB for the whole input range. The closed-loop bandwidth and the phase margin are 192 MHz and 76 degrees, respectively. The total integrated noise at output is 9.72 μV^2, and then the input referred integrated noise is $0.179\mu V^2$. The OPAMP consumes a DC power of around 264 μW.

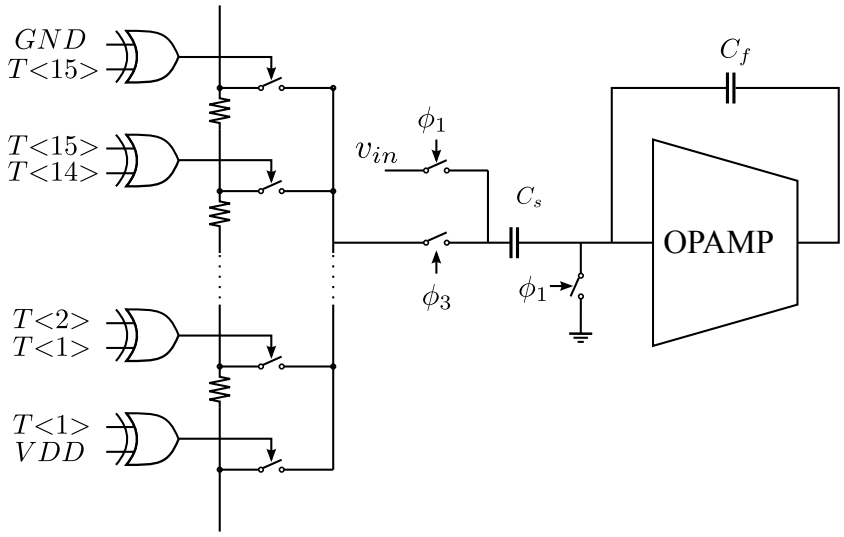

Figure 2.9: The 4-bit DAC and the subtracter.

2.5.4 Delay-line ADC

In this subsection, we will discuss the second stage delay-line ADC. The delay cell is the core of the delay line ADC, which determines the speed and the resolution of the delay line ADC. The delay cell used in this work is the dual-input delay cell (DIDC), and the delay line is a weight-adjusted DIDC chain [37]. Figure 2.11 shows the diagram of DIDC and a weight-adjusted DIDC chain. Each DIDC with size $M : 1$ generates an extra virtual input with ratio $M : 1$ between two input, in_1 and in_2, shown in Figure 2.12. The output time is the intrinsic delay of the DIDC, $\widetilde{D}_0$, plus the time of the extra virtual input. Thus, we can derive the delay between in_2 and out, $\widetilde{D}_{in2\rightarrow out}$ as follows.

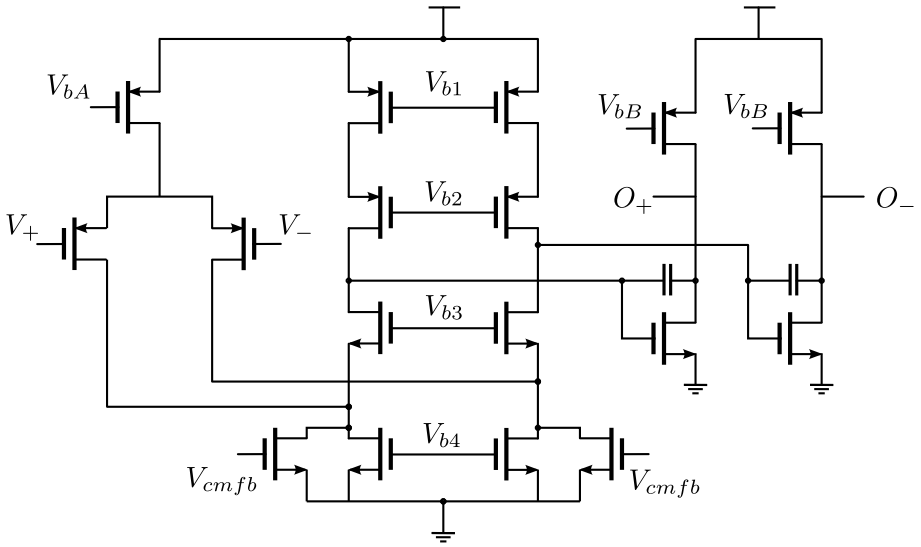

Figure 2.10: The operational amplifier in the subtracter.

$$\widetilde{D}_{in2\to out} = \widetilde{D}_0 - \left(\frac{1}{M+1}\right)\widetilde{D}_{in1\to in2}$$

For a weighted-adjusted DIDC chain, where the sizes of all delay cells are "$M:1$", the delay of the n-th delay cell, $\widetilde{D}_n$ can be written as follows.

$$\widetilde{D}_n = \widetilde{D}_0 - \left(\frac{1}{M+1}\right)\widetilde{D}_{n-1}$$

The closed form of $\widetilde{D}_n$ is shown as follows.

$$\widetilde{D}_n = \widetilde{D}_0\left[\left(\frac{M+1}{M+2}\right) + \frac{1}{M+2}\left(\frac{-1}{M+1}\right)^{n-1}\right]$$

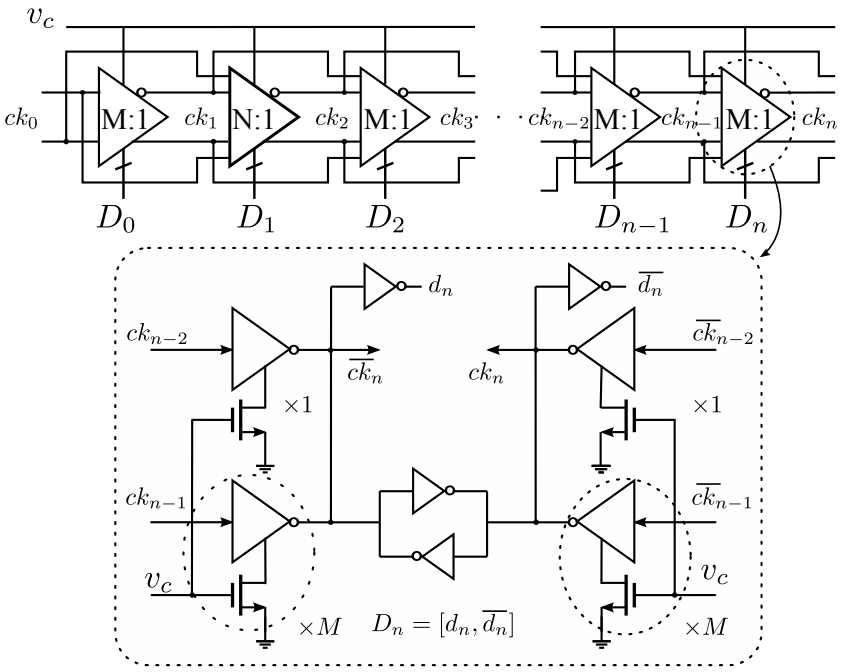

Figure 2.11: DIDC and weight-adjusted DIDC chain.

$\widetilde{D}_n$ converges to $(M+1)/(M+2)\widetilde{D}_0$. If the second delay cell uses size "$N:1$" instead of $M:1$, where $N = M+1$, $\widetilde{D}_2 = (M+1)/(M+2)Delay_0$, which is the same with the final settled delay. Thus, a constant-delay characteristic can be derived starting from the second delay cell, which can improve the linearity of the delay line. In this work, we use $M = 1$ and $N = 2$. In the simulation results, without any calibration technique, SNDR is 28.7 dB with sampling rate 312.5 MHz, shown in Figure 2.3.

Figure 2.13 illustrates the block diagram of the second stage delay-line ADC. First, the S/H circuit samples the differential outputs of the subtracter, O_+ and O_-, and then the sampled signals are used to control the delay of the

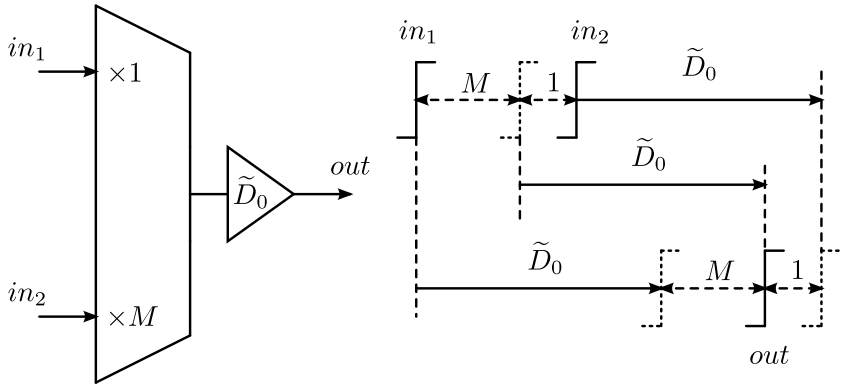

Figure 2.12: DIDC with wight of $M : 1$.

delay cells. Finally, the number of delay cells the signal passes through is the quantization result.

2.6 Simulation results

The proposed hybrid ADC is designed and simulated in a commercial 65 nm CMOS process. Table 2.1 summarizes the simulation results. It consumes 1.6mW, and Table 2.2 shows the power consumption in each building block. The differential non-linearity (DNL) and integral non-linearity (INL) are shown in Figure 2.14, and the ranges of DNL and INL are 0.47/-0.2 LSB and 0.52/-0.6 LSB, respectively. The high frequency simulation is done by applying a 43 MHz sinusoidal input. Figure 2.15 illustrates the spectrum of the simulation result. The signal-to-noise-plus-distortion ratio (SNDR) and the spurious free dynamic range (SFDR) are 55.6 dB and 68.5 dB, respectively, which amounts to an effective number of bits (ENOB) = 8.94 bits.

Figure 2.16 shows the power and noise contributions of the proposed

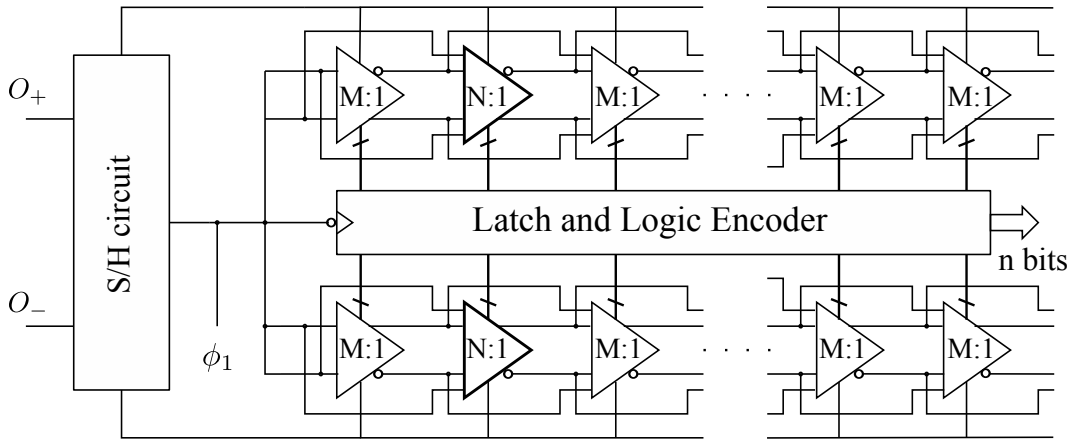

Figure 2.13: Delay-line ADC structure using DIDC.

hybrid ADC. Figure 2.16(a) illustrates that the 4-bit flash ADC including the 4-bit DAC, the residue amplifier and the delay-line ADC contributes 60%, 16%, and 24%, respectively. Figure 2.16(b) depicts that noise is mainly contributed from the quantization noise and the noise of the residue amplifier of the first-stage ADC. It can be seen that the first-stage ADC consuming 76% of the power contributes 75% of the noise, while the second-stage delay-line ADC consuming 24% power contributes of the 25% noise.

To compare the hybrid ADC to other work in terms of power consumption, sampling rate, and resolution, the figure of merit (FOM) defined in [42] is used.

$$\text{FOM} = \frac{Power}{2^{\text{ENOB}} \times \min(2f_{\text{in}}, f_{\text{sample}})}$$

The FOM of the proposed hybrid ADC is 33.8 fJ/conversion-step at 96MS/s and a 1.1 V supply. Table 2.3 shows the comparison between the proposed

Technology	65 nm CMOS
Supply Voltage	1.1 V
Sampling Rate	96 MS/s
Number of Bits	11
Differential input range	0.8 V p-p
SNDR @ 43 MHz	55.6 dB
SFDR @ 43 MHz	68.5 dB
Power Consumption	1.6 mW

Table 2.1: Performance summary of the hybrid ADC.

	Flash ADC + DAC	Subtractor	Delay-line ADC
Power (μW)	956	264	380

Table 2.2: Power consumption of the components.

hybrid ADC and other state-of-the-art ADCs [3, 5, 10, 26, 43, 47]. It shows that the hybrid ADC can achieve a competitive FOM with other state-of-the-art ADCs.

2.7 Conclusion

In this chapter, we proposed a novel 11-bit hybrid ADC, consisting of a 4-bit flash ADC followed by a 7-bit delay-line ADC. In this structure, the error/noise in the second stage 7-bit delay line ADC is significantly attenuated in the overall output. In the simulation results, the hybrid ADC yields a FOM

Reference	[10]	[3]	[47]	[26]	[5]	[43]	This work
Architecture	Pipelined	Pipelined	SAR	SAR	Pipelined	Pipelined SAR	Hybrid
Technology	90nm	65nm	65nm	65nm	65nm	40nm	65nm
Supply Voltage (V)	1.2	1.2	1.0	1.2	1.0	1.1	1.1
Sampling Rate (MS/s)	100	100	50	100	200	250	96
Resolution (bit)	12	10	10	10	10	11	11
SNDR (dB)	63.2	59.0	56.6	56.0	57.0	56.0	55.6
Power (mW)	6.2	4.5	0.82	1.13	5.37	1.7	1.6
FOM (fJ/Conv.-step)	52.7	61.8	27.7	15.5	46.4	13.2	33.8

Table 2.3: Performance comparison of state-of-the-art work.

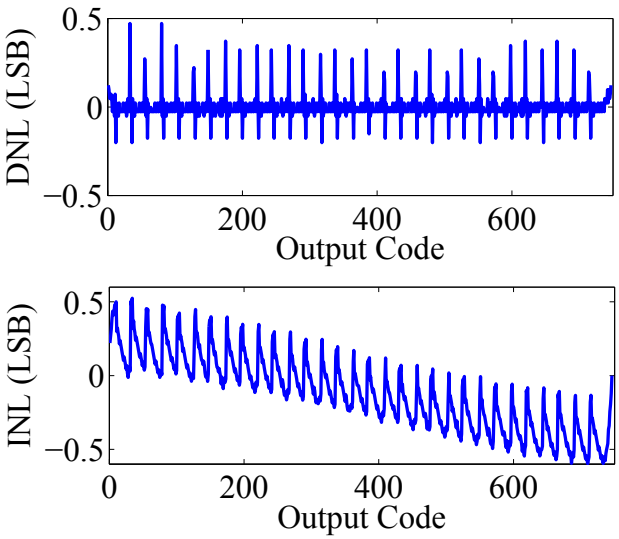

Figure 2.14: Simulated DNL and INL.

of 33.8 fJ/conversion-step, which is competitive with other state-of-the-art ADCs. The overall performance is not limited by the linearity issue of the delay-line ADC.

The design trade-offs for each building block of the hybrid ADC are discussed below. The guidelines about power/resolution trade-off are provided in the following.

- Adding an extra bit of flash ADCs costs 8x in power. For each extra bit in flash ADCs, the transistor width needs to be increased by 4x to maintain the same matching among comparators. Also, the number of transistors increases by 2x. Thus, an extra bit results in a power increment of 8x.

- Adding an extra bit of flash ADC reduces the power of the residue amplifier by half, which is explained as follows. From Equation 2.7, the

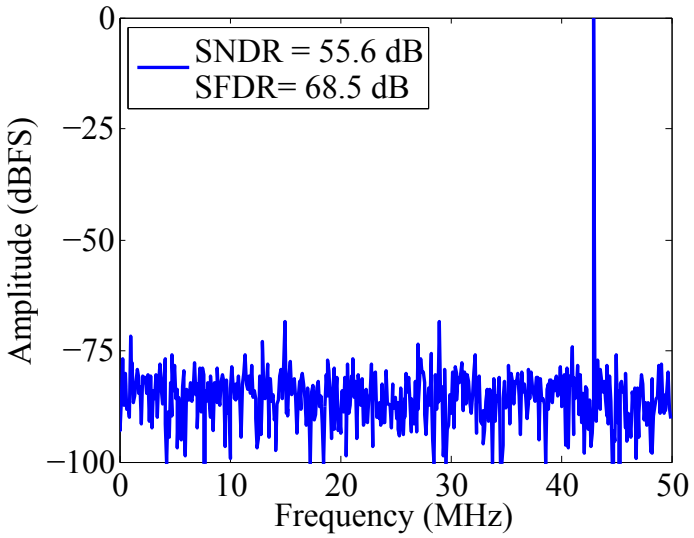

Figure 2.15: Output spectrum of a 43 MHz sinusoid input.

noise is proportional to $1/\beta$. When the number of bits of the flash ADC is increased by 1, β is increased by 2x, and noise will be reduced by half. It follows that power will also be reduced by half.

- Increasing the length of delay-line ADCs by 2x consumes 2x more power. In Figure 2.5, the operation time of the delay-line ADC is relatively small in a cycle. Increasing the operation time of the delay-line ADC results in more power consumption.

Figure 2.17 shows the normalized power of the 11-bit hybrid ADC with various partitions in number of bits used in the flash ADC and delay-line ADCs. It indicates that the hybrid ADC with either 3-bit or 4-bit flash ADC would have a better performance. Figure 2.18 illustrates the normalized power of the hybrid ADC with different resolutions. For a given resolution, the blue

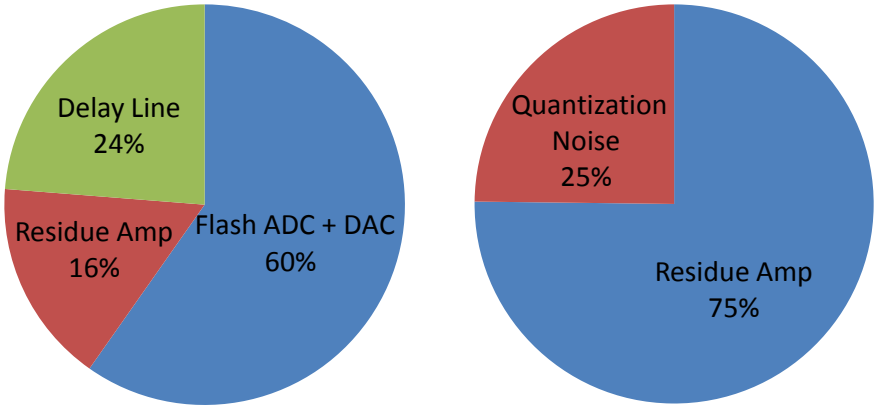

Figure 2.16: (a) Power contributions and (b) noise contributions of the proposed hybrid ADC.

line shows the normalized power when the number of the bits of the flash ADC changes from 3 to 5 with the 7 bit delay-line ADC, while the red line depicts the normalized power when the number of the bits of the delay-line ADC varies from 6 to 8 with the 4-bit flash ADC. It suggests that to increase the overall resolution, increasing the number of bits of the delay-line ADC is more power efficient. On the other hand, to reduce the overall resolution, reducing the number of bits of the flash ADC is more power efficient.

Furthermore, the proposed ADC inherits accuracy and power efficiency from the flash ADC and the delay-line ADC, respectively. The advantages of the Hybrid ADC are listed in the following.

- Compared with flash ADCs, the proposed hybrid ADC can achieve higher resolution in a more power-efficient way. This is because increasing an extra bit of the flash ADC costs 8x in power, while in the proposed hy-

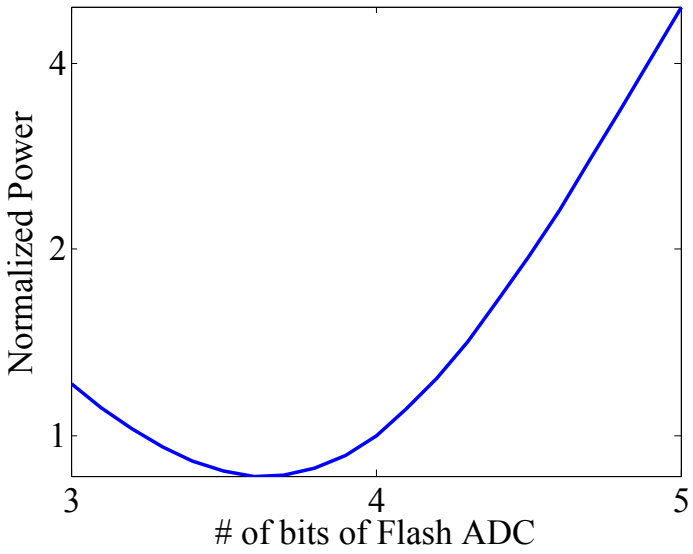

Figure 2.17: The normalized power of the 11-bit hybrid ADC with different resolution partitions.

brid ADC, this extra bit can be placed in the delay-line ADC which only costs 2x increment in power.

- Compared with delay-line ADCs, the hybrid ADC can operate at a higher speed. A 10-bit delay-line ADC can only run at a 25 MHz sampling rate, assuming that the delay per cell is $\sim$ 40 ps. The proposed hybrid ADC, however, can run at $\sim$ 100 MHz sampling rate using the same delay cells.

However, the hybrid ADC has some limitations. For example, delay cells are sensitive to process variation, a residue amplifier is needed, and the input range is critical to delay-line ADCs. These are discussed in the following.

- Delay cells are sensitive to process variation. In Section 2.8, the impact of mismatch of the delay-line ADC due to process variation is discussed.

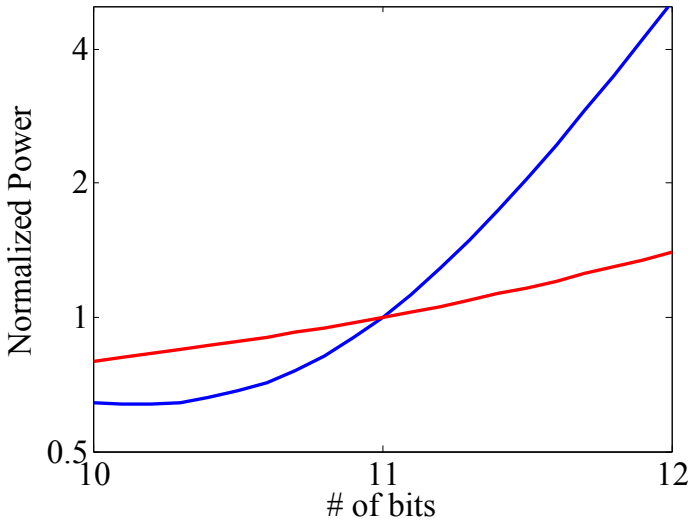

Figure 2.18: the normalized power of the hybrid ADC with different resolutions.

In different process corners, the delay per cell may have a 10% difference. This causes a gain error in the second-stage delay-line ADC such that the overall performance degrades.

- A residue amplifier is still needed, which cannot be scaled well with process advances.
- The input range is critical to delay-line ADCs. A large input range may cause harmonic distortion. A small input range requires a longer conversion time to achieve the same resolution.

With the advances in technology scaling, errors caused by process variation and distortions can be mitigated by calibration. Requirements for the residue amplifier can also be potentially relaxed when calibration is applied.

Scaling Parameter	SNR-Limited	Matching-Limited	Delay-line Circuits
Dynamic Range	$\propto \sqrt{C/kT}$	$\propto \sqrt{WL}$	Word length
Supply Voltage	$1/S$	$1/S$	$1/S$
Speed	1	1	S
Power	S	$1/S^2$	$1/S^2$

Table 2.4: Scaling of Mixed-Signal Circuits [7].

Table 2.4 shows the impact of scaling on mixed-signal circuits [7]. With process advances, device parameters are affected. When channel length shrinks, oxide thickness needs to become thinner in order to maintain the same control for the gate terminal over the channel. Consequently, supply voltage needs to be reduced to prevent gate oxide from breakdown. Therefore, technology scaling influences the performance of both analog and digital circuits. A flash ADC, a residue amplifier and a delay-line ADC are 3 main building blocks in the proposed hybrid ADC, and they belong to the matching-limited, SNR-limited, and digital circuit scaling scenarios in Table 2.4, respectively. Delay-line ADCs completely benefit from technology scaling in terms of power and speed, while flash ADCs can only reduce their power due to matching among comparators. Also, by the use of calibration as discussed above, the design of the residue amplifier is relaxed and its power consumption can be reduced. Therefore, the overall power and speed can be improved with technology scaling.

2.8 Appendix: mismatch of the delay-line ADC due to PVT variation

The PVT variation may cause a gain error in the second-stage delay line ADC. In this analysis, we assume that the first-stage ADC is ideal. With a gain error, b_1, the quantization result of the delay line ADC, x_2 can be simplified as follows.

$$x_2(v_{in}) = b_1 v_{in} + b_3 v_{in}^3 + e_2$$

In Figure 2.2, we know that the input of the delay-line ADC, $v'_{in} = 8e_1$. Thus, the quantization result, x_2 can be written as follows.

$$x_2(v'_{in}) = 8b_1 e_1 + 8^3 b_3 e_1^3 + e_2$$

Then, the overall output, x_{out} can be derived as follows.

$$\begin{aligned} x_{out}(v_{in}) &= v_{in} + (1-b_1)e_1 + 8^2 b_3 e_1^3 + e_2/8. \\ &= v_{in} + (1-b_1)e_1 + 4 \times 8^2 \times b_1 \times \text{HD3} \times e_1^3 + e_2/8 \end{aligned}$$

where HD3 $= \frac{1}{4} \times \frac{b_3}{b_1} = -29$ dB. Thus, we know that the resolution at the output is limited by the gain error of the second-stage ADC, $NS_0 = (1-b_1)e_1$, the harmonic distortion of the second-stage ADC, $NS_1 = 256 \times b_1 \times \text{HD3} \times e_1^3$, and the quantization noise of the second-stage ADC, $NS_2 = e_2/8$. Normally, $b_1 \approx 1$. However, the process variation may result in $b_1 \neq 1$. But, we can still adjust $m = N_T(\max(v_{in})) - N_T(\min(v_{in}))$ so that $b_1 \approx 1$. Then, we can derive the same result of x_{out} as Equation 2.9 as follows.

$$x_{out}(v_{in}) \quad = \quad v_{in} + 256 \times \mathrm{HD3} \times e_1^3 + e_2/8$$

Table 2.5 shows the simulation results in 3 different process corners and temperatures 27^{o}C and 70^{o}C. With the temperature and process variation, the SNDR may have a 10 dB decrement. Nonetheless, with a pre-calibration of the m-value adjustment, the SNDR only changes within 1 dB. Therefore, with the m-value adjustment, the impact of the process and temperature variations can be significantly reduced.

	T = 27^{o}C		T = 70^{o}C	
	SNDR w.o. m adjust.	SNDR with m adjust.	SNDR w.o. m adjust.	SNDR with m adjust.
Nominal	55.2 dB	55.2 dB	54.6 dB	55.2 dB
Weak	45.8 dB	54.4 dB	51.0 dB	56.1 dB
Strong	47.6 dB	55.8 dB	46.5 dB	54.8 dB

Table 2.5: Performance summary of the hybrid ADC in different process corners and temperatures.

Chapter 3

Digital Calibration for a Delay Line ADC Using Harmonic Distortion Correction

3.1 Background

With continued advances in integrated circuit fabrication technology, operation speed, area, and power have been significantly improved. Meanwhile, many accompanying complex effects impede analog circuit scaling [16, 21, 24]. In addition, voltage scaling causes noisier signals, and the relatively high threshold voltage squeezes the available signal headroom in a sophisticated analog design. The increased density and speed of the transistors can, however, be exploited by using digital calibration to improve the precision of analog circuits. Digitally supported analog is now becoming a mainstream design practise, and can be viewed as a powerful "design-for-test" methodology for analog circuits, for use both after manufacturing and in the field [21]. Therefore, a digital calibration technique is discussed to remove the noise/error of delay-line ADCs in this chapter.

Digital calibration techniques have been widely used to estimate and cancel error/distortion in pipeline ADCs [9, 29, 30, 35]. In [9], the least mean square method was used to digitally measure error of pipelined ADCs. In [35],

The project is supervised by Jacob A. Abraham. [21] H.-C. Lee and J. A. Abraham, "Digital Calibration for 8-bit Delay Line ADC Using Harmonic Distortion Correction," Asian Test Symposium (ATS), pp. 128 – 133, 2013

a digital calibration technique was proposed to estimate the gain error of amplifiers in a pipelined ADC. Finally, Panigada and Galton presented a digital background calibration technique, called harmonic distortion correction (HDC), to measure distortion introduced by residue amplifiers in pipelined ADCs and cancel it [29, 30].

In order to improve the linearity of delay-line ADCs, we extend HDC to digitally measure and cancel the gain error and the third harmonic distortion of a delay line ADC, since the simulation results show that the signal-to-noise-plus-distortion ratio (SNDR) of the delay line ADC is limited by the third harmonic distortion. The simulation results show that HDC, which significantly improves SNDR from 25.6 dB to 42.5 db by averaging 2^{27} points which corresponds to a 0.86 second calibration time, strongly supports the scalability of delay line ADCs and their improved performance in further scaled fabrication processes.

The remainder of this chapter is organized as follows. Section 3.2 discusses the noise and distortion analysis of delay-line ADC. Details of our digital calibration technique are discussed in Section 3.3, and convergence time analysis is described in Section 3.4. Section 3.5 gives the simulation results. Finally, the concluding remarks are given in Section 3.6.

3.2 Noise and Distortion of Delay Line ADCs

To illustrate the noise and distortion of delay-line ADCs, we consider the first three harmonic distortions introduced by the delay line ADC, since Figure 3.1 also shows that the first three harmonic distortions of the delay line ADC limit the overall resolution, while other harmonics except the fifth harmonic distortion are under the noise floor. In addition, the fifth harmonic

distortion would not limit the overall performance even when the third harmonic distortion is completely removed, since the total of other noise (-45.6 dBFS) is larger than the fifth harmonic distortion (-50.1 dBFS). Note that, although in Figure 3.1 the second harmonic distortion does not limit the overall performance, delay line ADCs digitize the input signal which includes a differential voltage and a common mode voltage. This section will discuss the impact of the common mode voltage on the first three harmonic distortions.

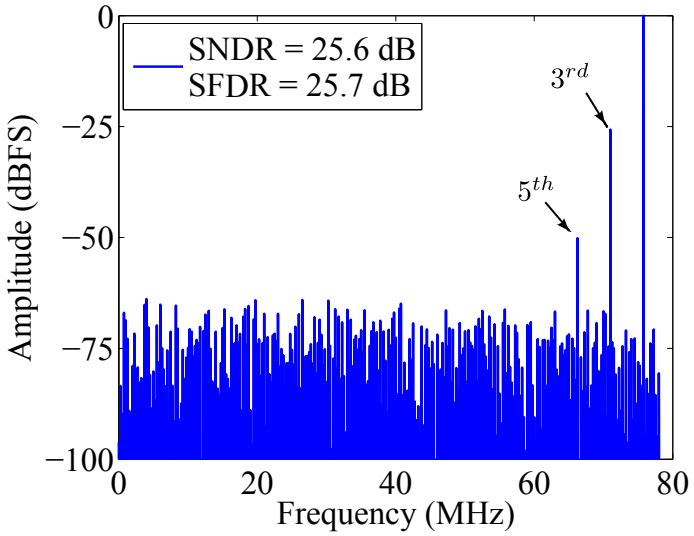

Figure 3.1: The spectrum of an 8 bit delay ADC.

Let f denote the distortion function, and f is defined as follows.

$$f(v) = a_1 v + a_2 v^2 + a_3 v^3$$

Then, the output of a delay line ADC is $v + a_1 v + a_2 v^2 + a_3 v^3 + e_q$, when applying input v, where e_q is the quantization noise. Let v_{cm} and v_d denote

the common mode voltage and the differential voltage of input. Then, the differential outputs, v_{o+} and v_{o-} can be expressed as follows.

$$\begin{aligned} v_{o+} &= v_{cm} + \frac{v_d}{2} + a_1(v_{cm} + \frac{v_d}{2}) + a_2(v_{cm} + \frac{v_d}{2})^2 \\ &\quad + a_3(v_{cm} + \frac{v_d}{2})^3 + e_{q+} \\ v_{o-} &= v_{cm} - \frac{v_d}{2} + a_1(v_{cm} - \frac{v_d}{2}) + a_2(v_{cm} - \frac{v_d}{2})^2 \\ &\quad + a_3(v_{cm} - \frac{v_d}{2})^3 + e_{q-} \end{aligned}$$

where e_{q+} and e_{q-} denote the quantization noise of the delay line with respect to v_{o+} and v_{o-}, respectively. Thus, the differential output, $v_o = v_{o+} - v_{o-}$ can be derived as follows.

$$\begin{aligned} v_o &= (1 + a_1)v_d + a_2(v_{cm} + \frac{v_d}{2})^2 + a_3(v_{cm} + \frac{v_d}{2})^3 \\ &\quad - a_2(v_{cm} - \frac{v_d}{2})^2 - a_3(v_{cm} - \frac{v_d}{2})^3 + e_q \end{aligned}$$

where e_q denotes the quantization noise of the differential delay line ADC. v_o can further be simplified as follows,

$$\begin{aligned} v_o &= (1 + a_1)v_d + 2a_2 v_{cm} v_d + 3a_3 v_{cm}^2 v_d + 2a_3(\frac{v_d}{2})^3 + e_q \\ &= v_d + \left((a_1 + 2a_2 v_{cm} + 3a_3 v_{cm}^2)v_d + \frac{a_3}{4} v_d^3\right) + e_q. \end{aligned}$$

Thus, we know the common voltage v_{cm} may degrade the input signal, but the second harmonic distortion can also be cancelled in differential delay line ADCs. Therefore, the distortion function can be simplified as follows.

$$f(v_d) \quad = \quad \alpha_1 v_d + \alpha_3 v_d^3 \tag{3.1}$$

which is a function of the differential voltage, v_d. Note that the effect of the common mode voltage, v_{cm} is formulated into α_1. Thus, if v is the differential input voltage of a delay line ADC, then its corresponding quantization result will be $v + f(v) + e_q = v + \alpha_1 v + \alpha_3 v^3 + e_q$.

In the next section, we will discuss the process of extracting α_1 and α_3 by extending HDC [29, 30], and then use the extracted coefficients to correct the error/distortion of delay line ADCs.

3.3 Details of Digital Calibration

Figure 3.2 is a diagram of the digital calibration technique. The differential inputs of the delay line ADC are $v_{i+}(nT_s)$ and $v_{i-}(nT_s)$ whose sampled values are $v[n]$ and $-v[n]$, respectively, where T_s denotes the sampling period. A set of 3 uncorrelated pseudorandom digital calibration sequences, $t_1[n]$, $t_2[n]$, and $t_3[n]$, each of which takes on values of $\pm A$, is zero-mean and independent of the input of the delay line ADC, is added to the input of the delay line ADC. Thus, during calibration, the two inputs of the delay line ADC are $v[n] + t_1[n] + t_2[n] + t_3[n]$ and $-v[n] - t_1[n] - t_2[n] - t_3[n]$, respectively. From Equation 3.1, we can derive the differential output of the delay line ADC which equals $2 \times [(1 + \alpha_1)\ (v[n] + t_1[n] + t_2[n] + t_3[n]) + \alpha_3(v[n] + t_1[n] + t_2[n] + t_3[n])^3] + e_q$. Thus, the input to digital calibration logic is

$$y[n] = (1 + \alpha_1)z[n] + \alpha_3(z[n])^3 + e_q/2 \tag{3.2}$$

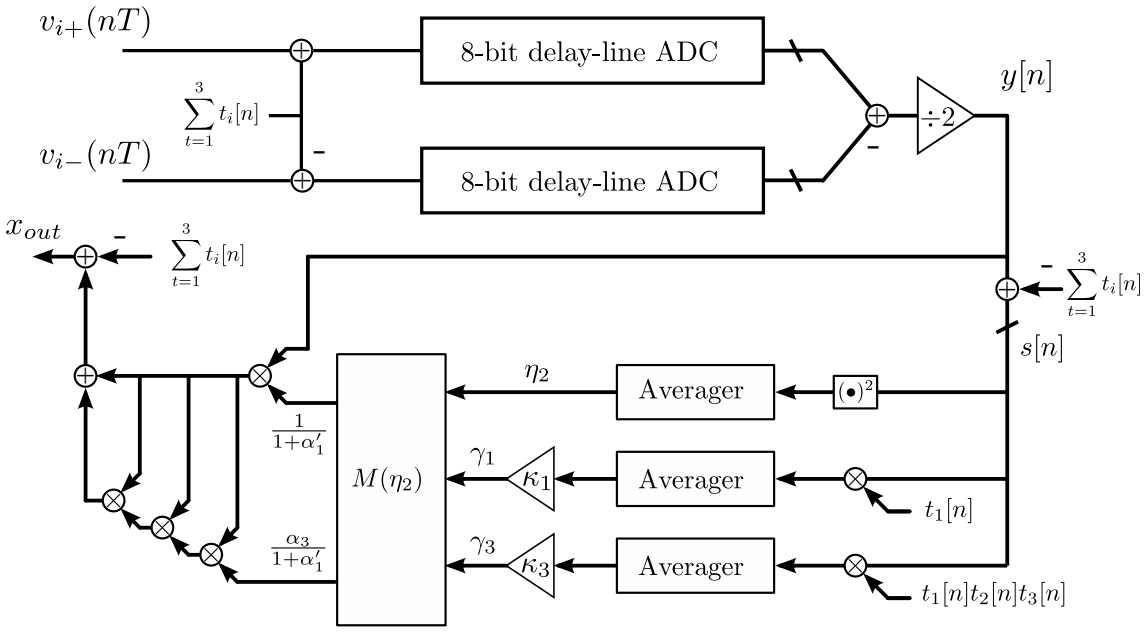

Figure 3.2: The digital calibration technique.

where $z[n] = v[n] + t_1[n] + t_2[n] + t_3[n]$.

The purpose of the digital calibration technique is to estimate $\alpha_1 z[n]$ and $\alpha_3(z[n])^3$, with which to cancel the linear and third-order distortions in the delay line ADC. To estimate α_1 and α_3, correlating $y[n]$ against the calibration sequences $t_1[n]$ and $t_1[n]t_2[n]t_3[n]$ are used, respectively. The correlation involves multiplying the digital sequence

$$s[n] = v[n] + \alpha_1 z[n] + \alpha_3(z[n])^3 + e_q/2$$

by $t_1[n]$ and $t_1[n]t_2[n]t_3[n]$ when estimating α_1 and α_3, respectively, since the calibration sequences $t_1[n]$, $t_2[n]$ and $t_3[n]$ are zero-mean, uncorrelated with each other, and independent of the delay line ADC input signal. Thus,

$t_1[n]t_2[n]t_3[n]$ is uncorrelated with all of the terms in $s[n]$ except the term $3! \times (t_1[n]t_2[n]t_3[n])\alpha_3$. Consequently, the average of $s[n] \times t_1[n]t_2[n]t_3[n]$ over n can be derived as follows.

$$\overline{s[n] \times t_1[n]t_2[n]t_3[n]} = 3! \times A^{2\times 3}\alpha_3$$

where A is the value of $|t_i[n]|$. The digital calibration logic multiplies $\overline{s[n] \times t_1[n]t_2[n]t_3[n]}$ by $\kappa_3 = A^{-2\times 3}/(3!)$ to obtain γ_3 which is an estimate of α_3. Then, γ_3 is multiplied by $(y[n])^3$ to obtain an estimate of $\alpha_3(v[n])^3$.

Similarly, $t_1[n]$ is uncorrelated with all of the terms in $s[n]$ except the terms $\alpha_1 t_1[n]$, $\alpha_3(t_1[n])^3$, $3\alpha_3 t_1[n](v[n])^2$, $3\alpha_3 t_1[n](t_2[n])^2$, and $3\alpha_3 t_1[n](t_3[n])^2$. Therefore, the average of $s[n] \times t_1[n]$ over n can be also derived as follows.

$$\overline{s[n] \times t_1[n]} = \alpha_1 A^2 + 7\alpha_3 A^4 + 3\alpha_3 A^2 \overline{(v[n])^2}.$$

After being multiplied by $\kappa_1 = A^{-2}$, $\gamma_1 = \kappa_1 \times \overline{s[n] \times t_1[n]}$ converges to $\alpha_1 + 7\alpha_3 A^2 + 3\alpha_3 \overline{(v[n])^2}$. An unwanted term $3\alpha_3 \overline{(v[n])^2}$ exists in $\overline{s[n] \times t_1[n]}$. $\eta_2 = \overline{(s[n])^2}$ is used to approximate $\overline{(v[n])^2}$. Therefore, the relation between estimates of α_1 and α_3, α_1' and α_3', and γ_1 and γ_3 can be found in the following.

$$\begin{bmatrix} \gamma_1 \\ \gamma_3 \end{bmatrix} = \begin{bmatrix} 1 & 7A^2 + 3\eta_2 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \alpha_1' \\ \alpha_3' \end{bmatrix}$$

Then, we can derive α_1' and α_3' as follows.

$$\begin{bmatrix} \alpha_1' \\ \alpha_3' \end{bmatrix} = \begin{bmatrix} 1 & -7A^2 - 3\eta_2 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \gamma_1 \\ \gamma_3 \end{bmatrix} \tag{3.3}$$

Therefore, the corrected quantization result of the delay line ADC, x_{out}, can be obtained as follows.

$$\begin{aligned} x_{out}[n] &= \frac{y[n]}{1+\alpha_1'} - \frac{\alpha_3'}{(1+\alpha_1')^4}(y[n])^3 - \sum_{i=1}^{3} t_i \\ &= v[n] - \frac{3\alpha_3'^2}{(1+\alpha_1')^2}(z[n])^5 \\ &\quad - \frac{3\alpha_3'^3}{(1+\alpha_1')^3}(z[n])^7 - \frac{\alpha_3'^4}{(1+\alpha_1')^4}(z[n])^9 \end{aligned} \tag{3.4}$$

where $z[n] = v[n] + t_1[n] + t_2[n] + t_3[n]$ and the quantization noise, e_q is not shown in the above equation.

From Equation 3.8, we know that the linear and third-order distortions have been removed, and the introduced fifth and higher order distortion terms in x_{out} are comparatively small and can be neglected.

As mentioned in [29, 30], HDC is a background calibration technique which estimates the linear and third harmonic distortion coefficients, α_1 and α_3 during normal operation of the ADC. In addition, the selection of the value of $|t_i|$, A significantly influences the convergence time of α_1 and α_3 and the correction result. Thus, in the simulation, A is set to $V_{FS}/50$, where $V_{FS} = \max(v_{in}) - \min(v_{in})$ which improves SNDR by 16.9 dB with only 2^{27} samples which corresponds to a 0.86 second calibration time.

3.4 Convergence time analysis

The convergence time analysis of HDC for the pipelined ADC calibration has been done by Panigada and Galton in [30] and the following illustrates briefly the convergence time analysis for the delay-line ADC calibration.

By the HDC logic, γ_i can be written as

$$\gamma_k = \frac{1}{k!A^kP}\sum_{i=0}^{P-1} s[i]c[i] \tag{3.5}$$

where

$$c[n] = \begin{cases} 1, & \text{if } t_1[n]t_2[n]...t_k[n] > 0 \\ -1, & \text{otherwise} \end{cases}$$

and P is the number of samples averaged by the averager blocks. If the averagers are ideal, γ_k would converge to its ideal value, $\gamma_k|_{\text{ideal}}$. However, P is finite in any practical averager, so the mean squared value of the estimation error, i.e., $\mathrm{E}\{(\gamma_k - \gamma_k|_{\text{ideal}})^2\}$, is used to quantify the estimation error. By the definition, $c[n]$ is a white random sequence with zero mean and unity variance, and independent of the input signal. With A set to V_{FS}/m, We can derive $\mathrm{E}\{(\gamma_k - \gamma_k|_{\text{ideal}})^2\}$ as follows.

$$\mathrm{E}\{(\gamma_k - \gamma_k|_{\text{ideal}})^2\} = \frac{1}{P}(\frac{m}{V_{\text{FS}}})^{2k}(\frac{1}{k!})^2\left(\frac{1}{P}\sum_{i=0}^{P-1} u^2[i]\right) \tag{3.6}$$

where m is a design parameter, and $u[n]$ equals $s[n]$ minus the terms that are correlated with $c[n]$. Since $V_{\text{FS}} > u[n]$, Equation 3.6 is a function of $1/P$, which has the form of a bounded sequence divided by P. Hence, as expected, it implies that the mean squared error goes to zero, when $P \to \infty$.

The required convergence time is the minimum value of P for which the HDC logic is able to measure all the α_k values with sufficient accuracy. Equation 3.6 gives insight into which terms affect the required converge time.

For example, the mean squared estimation error for a given P gets worse as m increases. But, a smaller m reduces significantly the dynamic range of the delay-line ADC and results in that $\overline{(s[n])^2}$ cannot be a good estimation of $\overline{(v[n])^2}$. Also, when k is increased, the mean squared estimation error for a given P gets worse. The simulation results also show that the convergence time of α_3 is much longer than the convergence time of α_1. Note that $\alpha_3 = \gamma_3$ and α_1 are derived directly from γ_1 and γ_3. The convergence time of γ_1 and γ_3 directly influence the convergence time of α_1 and α_3. However, a closed-form expression for the required convergence time is unknown. Hence, the m value and the required convergence time are determined by computer simulation on a case-by-case basis.

3.5 Simulation results

In order to demonstrate the calibration result of a delay-line ADC using the harmonic distortion correction technique, a delay line ADC with 256 delay cells is implemented and simulated in a commercial 65nm process. Figure 3.3 illustrates the block diagram of the delay line ADC used in this work. First, the S/H circuit samples the differential inputs v_{i+} and v_{i-}. After adding pseudo random numbers, $\sum_{i=1}^{3} t_i$ by a switched-capacitor circuit, the differential signals to the delay-line are $v_{i+} + \sum_{i=1}^{3} t_i$ and $v_{i-} - \sum_{i=1}^{3} t_i$, which are used to control the delay of the delay cells. Finally, the delay line quantizes input to the digital quantization result, which is the number of delay cells the signal passes through. Note that the S/H circuit is a switched-capacitor circuit with a bootstrapped switch [2] which can maintain the on-resistance of the switch at a small value, such that the switch linearity is improved.

The delay cell is the core of the delay line ADC, which determines

Technology	65nm CMOS
Supply Voltage	1.1V
Sampling Rate	156.25MS/s
Length of delay line	256 cells
Differential input range	0.8V p-p
SNDR@75MHz	25.6 dB
SFDR@75MHz	25.7 dB
Power	0.98 mW

Table 3.1: The summary of the simulation result without enabling harmonic distortion correction.

the speed, and the resolution of the delay line ADC. The delay cell used in this work is the dual-input delay cell (DIDC), and the delay line is a weight-adjusted DIDC chain [37]. The details of the DIDC are described in Section 2.5.4.

Table 3.1 shows the summary of the simulation results before enabling the digital calibration technique. The sampling rate is 156.25 MHz, and the differential peak-to-peak input range is 0.8 volt. The high frequency simulation is done by applying a 75 MHz sinusoid wave. SNDR is 25.6 dB, while SFDR is 25.7 dB. Figure 3.4(a) shows the spectrum of the delay line ADC before enabling the digital harmonic distortion correction. The overall performance is limited by the third harmonic distortion.

Figure 3.4(b) shows the spectrum of the delay line ADC after enabling the digital harmonic distortion correction. Compared with the spectrum before correction, the third harmonic distortion is significantly reduced. SNDR and

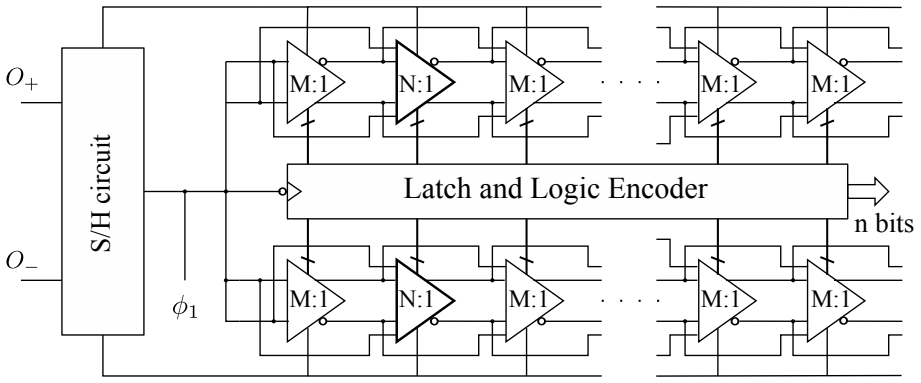

Figure 3.3: Delay-line ADC structure using DIDC.

SFDR are drastically improved to 42.5 dB and 45.4 dB, respectively. Note that in Figure 3.4(b), the fifth harmonic distortion does not limit the overall performance, since SNDR without considering the fifth harmonic distortion is 42.5 dB. Therefore, removing the fifth harmonic distortion would not further improve the overall SNDR.

Figure 3.5 shows the plot of the simulated SNDR and SFDR vs. the number of points averaged in the harmonic distortion correction. The extracted α_1 and α_3, generated by averaging more than 2^{26} points and used to calibrate the delay-line ADC, can achieve a SNDR more than 40 dB. It suggests the minimum number of averaged points to achieve a SNDR more than 40 dB is 2^{26} which corresponds to approximately 0.43 second calibration time. Figure 3.6 illustrates the plot of the figure of merit (FOM) vs. the number of points averaged. FOM is a quantity used to characterize the performance of ADCs in terms of power consumption, sampling rate and resolution, and defined as follows [42].

	T=27^{o}C		T=70^{o}C	
	SNDR (2^{29})	Conv. SNDR	SNDR (2^{29})	Conv. SNDR
Nominal	$>$ 40 dB	40.86 dB	$>$ 37 dB	38.52 dB
Weak	$>$ 39 dB	39.03 dB	$>$ 39 dB	40.63 dB
Strong	$>$ 36 dB	38.16 dB	$>$ 34 dB	35.01 dB

Table 3.2: The SNDR after taking more than 2^{29} averaging points and the convergence SNDR when taking 2^{37} averaging points at temperatures, 27^{o}C and 70^{o}C, with different corners.

$$\text{FOM} = \frac{Power}{2^{\text{ENOB}} \times \min(2f_{\text{in}}, f_{\text{sample}})}$$

In Figure 3.6, after averaging 2^{27} samples, the FOM is greatly improved from 403.0 fJ/conversion-step to 57.8 fJ/conversion-step which compares well with most state-of-the-art ADCs. Note that the power calculation does not include the power of the digital calibration, but the power of the calibration is much less than the power of the delay line ADC, since the calibration circuitry is digital.

Furthermore, in real applications, the input signal would not be a pure sinusoidal wave, and different random inputs may result in different calibration results. Figure 3.7 shows the SNDR histogram of enabling the harmonic distortion correction after taking 2^{29} averaging points, where the mean is 40.22 dB, and the variance is 4.67. This indicates that, with different inputs, HDC can also cancel distortions greatly. Also, the speed of cells may be different due to temperature and process variations. Thus, a random signal is injected

at the input and simulated with different process corners and different temperatures. Table 3.2 shows the SNDR after taking more than 2^{29} averaging points and the convergence SNDR when taking 2^{37} averaging points at temperatures, 27^oC and 70^oC, with different corners. It shows that HDC can still remove distortions effectively at different temperatures and different process corners.

3.6 Conclusion

In this chapter, we extend the harmonic distortion correction technique for the calibration of a delay line ADC. In the simulation results, calibration can achieve a SNDR of 42.5 dB and a SFDR of 45.4 dB, compared with the original SNDR of 25.6 dB and the original SFDR of 25.7 dB. Therefore, with the harmonic distortion correction, a delay-line ADC can easily obtain an effective number of bits greater than 4 bits, since current reported delay line ADCs can barely obtain a resolution of more than 4 bits. This technique strongly supports the scalability of delay line ADCs and their improved performance in further scaled fabrication processes.

3.7 Appendix: Mismatch analysis

In this section, the mismatch analysis is given, since mismatch may occur in long delay lines. Let f_1 and f_2 denote the distortion function of two delay lines, respectively, and f_1 and f_2 are defined as follows.

$$\begin{aligned} f_1(v) &= a_0 + a_1 v + a_2 v^2 + a_3 v^3 \\ f_2(v) &= b_0 + b_1 v + b_2 v^2 + b_3 v^3 \end{aligned}$$

Thus, the differential outputs of the delay-line ADC, v_{o+} and v_{o-}, equal $a_0 + v + a_1 v + a_2 v^2 + a_3 v^3$ and $b_0 - v - b_1 v + b_2 v^2 - b_3 v^3$, respectively.

Then, we can derive the output of the delay-line ADC as follows.

$$\begin{aligned} v_{o+}(v) - v_{o-}(-v) &= (a_0 - b_0) + 2v + (a_1 + b_1)v + (a_2 - b_2)v^2 \\ &+ (a_3 + b_3)v^3 \end{aligned} \quad (3.7)$$

From Equation 3.7, we know that the mismatch between two delay lines introduces an offset and second harmonic distortion, which cannot be removed by the digital calibration technique described in Section 3.3. From Equation 3.7, we know that

$$\begin{aligned} \overline{v_{o+}(0) - v_{o-}(0)} &= a_0 - b_0 \\ \overline{v_{o+}(v) - v_{o-}(-v)} &= (a_0 - b_0) + (a_2 - b_2)\overline{v^2} \end{aligned}$$

We can obtain that

$$\begin{aligned} a_0 - b_0 &= \overline{v_{o+}(0) - v_{o-}(0)} \\ a_2 - b_2 &= \frac{\overline{v_{o+}(v) - v_{o-}(-v)} - \overline{v_{o+}(0) - v_{o-}(0)}}{\overline{v^2}} \end{aligned}$$

where $\overline{v^2}$ can be estimated by $\overline{y^2}$. During correction, where the calibration sequences t_1, t_2, and t_3 are injected, we can first remove the offset , $a_0 - b_0$, and derive that the input to digital logic equals

$$y[n] = (1 + \alpha_1)z[n] + \alpha_2(z[n])^2 + \alpha_3(z[n])^3 + e_q/2$$

where $z[n] = v[n] + t_1[n] + t_2[n] + t_3[n]$, $\alpha_1 = (a_1 - b_1)/2$, $\alpha_2 = (a_2 - b_2)/2$, and $\alpha_3 = (a_3 - b_3)/2$. As discussed in Section 3.3, when estimating α_1 and α_3, $\overline{s[n] \times t_1[n]}$ and $\overline{s[n] \times t_1[n]t_2[n]t_3[n]}$ are used. Considering mismatch between the delay lines, $s[n]$ equals

$$s[n] = v[n] + \alpha_1 z[n] + \alpha_2 (z[n])^2 + \alpha_3 (z[n])^3 + e_q/2$$

We know that $\alpha_2(z[n])^2$ is uncorrelated with $t_1[n]$ and $t_1[n]t_2[n]t_3[n]$, so we can derive

$$\begin{aligned} \overline{s[n] \times t_1[n]t_2[n]t_3[n]} &= 3! \times A^{2\times 3}\alpha_3 \\ \overline{s[n] \times t_1[n]} &= \alpha_1 A^2 + 7\alpha_3 A^4 + 3\alpha_3 A^2 \overline{(v[n])^2}. \end{aligned}$$

which are the same as that without considering match. Therefore, the digital calibration technique can still be applied to estimate and remove the gain error and the third harmonic distortion. For the correction scheme, we use

$$x_{out}[n] = \frac{y[n] - \alpha_2 \eta_2}{1 + \alpha_1'} - \frac{\alpha_3'}{(1 + \alpha_1')^4}(y[n])^3 - \sum_{i=1}^{3} t_i$$

where $\alpha_2 = (a_2 - b_2)/2$, and $\eta_2 = \overline{(s[n])^2}$. Therefore, with considering mismatch, the harmonic distortions can also be reduced significantly.

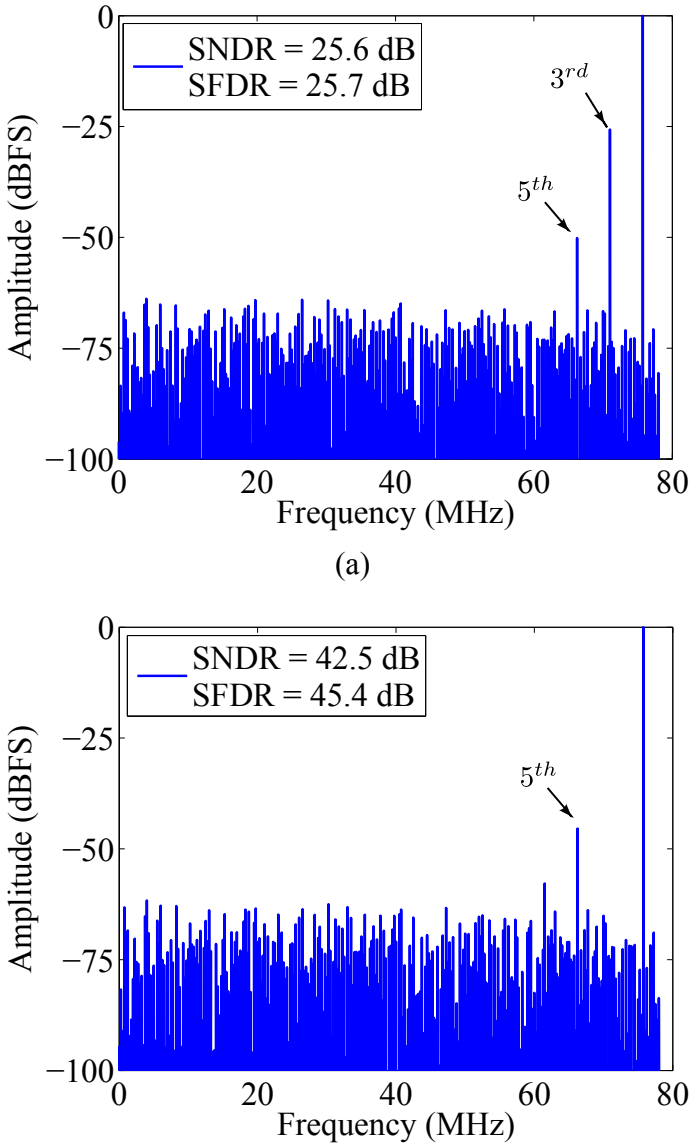

Figure 3.4: The spectrum of the delay line with a 75 MHz sinusoid input (a) before enabling digital harmonic distortion correction and (b) after enabling digital harmonic distortion correction.

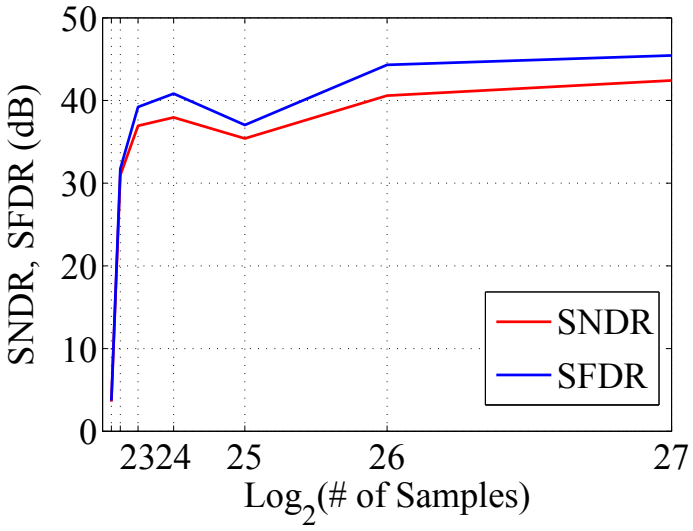

Figure 3.5: Simulated SNDR and SFDR versus the number of points averaged in the harmonic distortion correction.

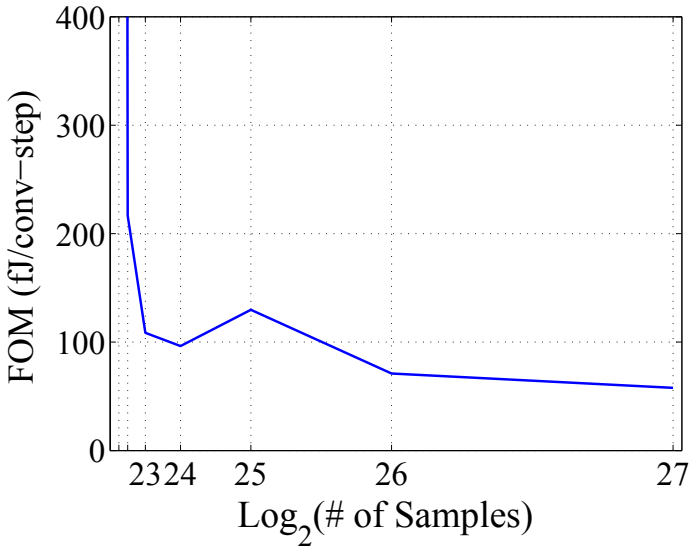

Figure 3.6: FOM versus the number of points averaged in the harmonic distortion correction.

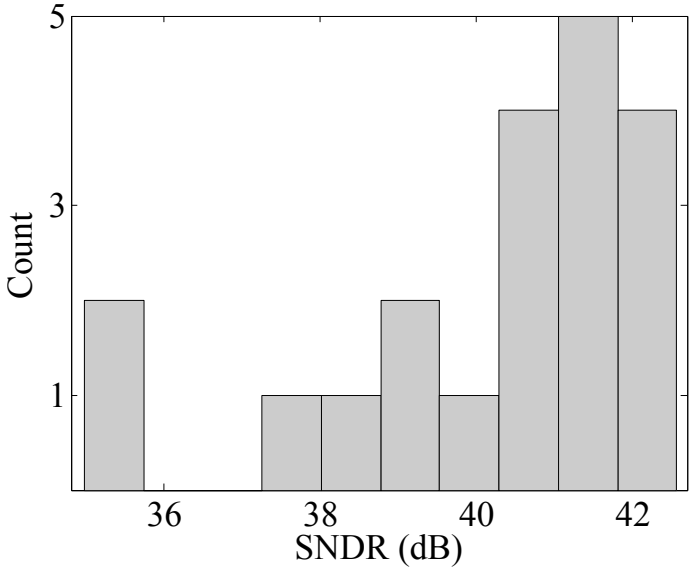

Figure 3.7: The SNDR histogram after taking 2^{29} averaging points.

Chapter 4

Multiple-Pass Delay-line ADC

4.1 Background

In this chapter, we present a multiple-pass delay-line ADC to improve the overall ADC performance in terms of resolution and speed. The multi-pass structure has been widely used in the phase-lock loop (PLL) [12]. The voltage-controlled-oscillator (VCO) is the most important component in the PLL. A CMOS VCO can be realized by ring structures, relaxation circuits or an LC resonant circuit. Ring oscillators are one of straightforward implementations which can provide multiple output phases and wide tuning ranges with less die area. In order to explore the maximum frequency levels of ring oscillators, several architectures, such as subfeedback loops [39], output-interpolation methods [38], multiple-feedback loops [19], and dual-delay paths [23, 31], are studied. The multiple-pass loop is one of the popular designs to improve the maximum frequency. Therefore, in this chapter, we introduce a delay-line ADC which uses the multiple-pass structure to improve the speed of delay cells and also a phase interpolation technique is employed to increase the number of the bits of the ADC. The prototype circuits were simulated in a commercial 40nm CMOS process, and achieved an SNDR 37dB with power consumption 4.2mW and 500 MHz sampling rate.

The remainder of this chapter is organized as follows. The multiple-pass delay line is discussed in Section 4.2. Section 4.3 illustrates the phase interpo-

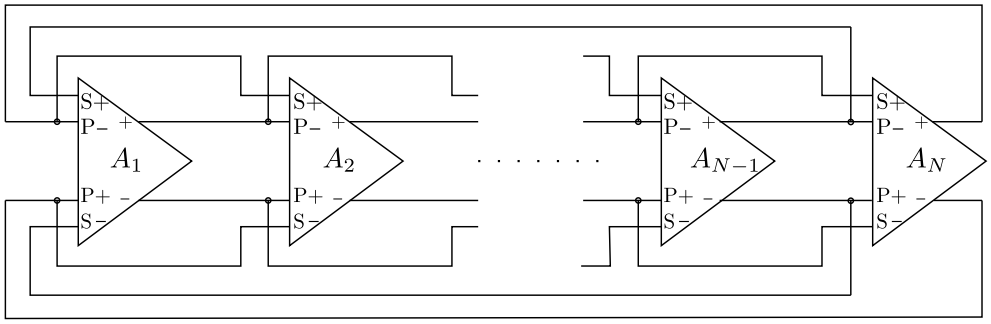

Figure 4.1: N-stage multiple-pass ring oscillator.

lation technique. Section 4.4 gives the simulation results. Finally, concluding remarks are given in Section 4.5.

4.2 Multiple-Pass Delay Line

As mentioned in the previous section, the multiple-pass loop is a popular structure to increase the maximum frequency of the ring oscillators in PLL. Figure 4.1 shows an N-stage ring with the multiple-pass loop structure. In this structure, an auxiliary feedforward path is added to accelerate the speed of each stage. A set of additional secondary inputs, S+ and S-, can be early triggered such that the delay of the delay cell is reduced and less than the minimum delay of the delay cells. The inputs from the previous stages are switched during the operation. In [12], a 5.9 GHz tuning frequency was achieved in a 0.18 μm CMOS process. This concept can be easily applied to the analog-to-digital conversion by breaking the ring into a delay line.

In this chapter, we present a delay line ADC which uses the multiple-pass structure. Figure 4.2 shows the proposed delay line. Two inverters are

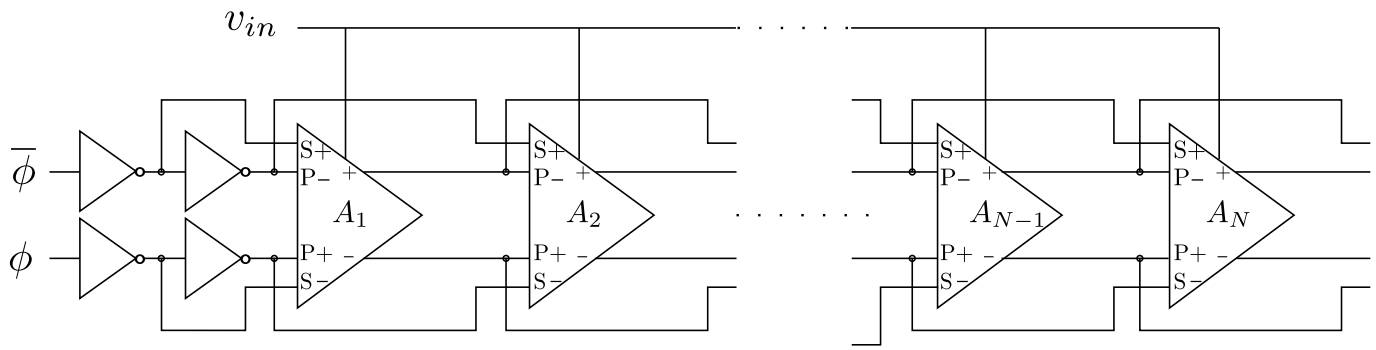

Figure 4.2: N-stage multiple-pass delay line.

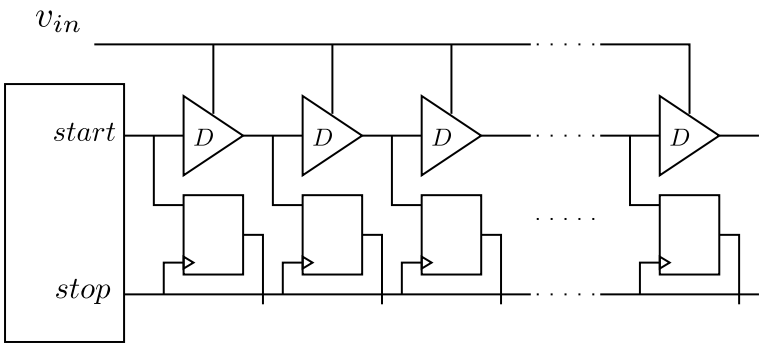

Figure 4.3: The diagram of voltage-to-delay-to-digital ADCs.

added in front of the multi-pass delay line, and the first two delay cells, A_1 and A_2 receive signals from the inverters. When a conversion starts, the signals, ϕ, $\overline{\phi}$, pass through inverters and then arrive the multiple-pass delay line. The first and second delay cells can also be pre-triggered by the outputs of inverters, such that the delay of the subsequent delay cells becomes stable quickly. The structure of the delay-line ADC used in this chapter is the voltage-to-delay-to-digital conversion, shown in Figure 4.3. In this structure, the quantization result is the number of the voltage-controlled delay cells a signal passed through in a given time, T. The number of bits is defined as follows.

$$R \approx \log_2 T|V_a - V_b| \times \left| \frac{1}{D^2(V)} \frac{dD(V)}{dV} \right|_{V=V^*} \tag{4.1}$$

where $[V_a, V_b]$ is the interest of the input voltage range, $D(V)$ is the delay per cell, and V^* is a constant in $[V_a, V_b]$ [24, 44]. Equation 4.1 shows that increasing T and the interest input range, $[V_a, V_b]$ can improve the number of bits, R. However, increasing T implies decreasing sampling rate, and extending the

input range, [V_a, V_b], causes a linearity issue. Thus, it is necessary to reduce $D(V)$ to improve the overall performance. Unfortunately, the delay of delay cells is limited by the process technology. The multiple-pass structure, on the other hand, provides a way to overcome the limit of the process technology. Also, phase interpolation is used in this work to improve the time resolution and is discussed in Section 4.3.

4.3 Phase Interpolation

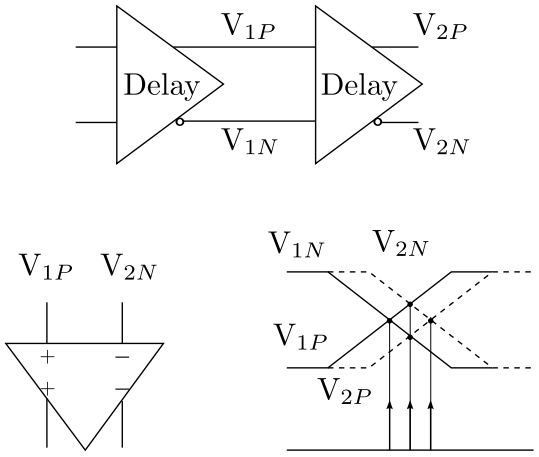

Figure 4.4: Single-ended to differential phase interpolation scheme

Phase interpolation is attractive and widely used in VCOs to increase the time resolution. A VCO with N differential delay cells has $2N$ phases. Phase interpolation technique can obtain more phases while the frequency is maintained. Figure 4.4 shows a single-ended to differential phase interpolation scheme [18]. Positive and negative signals are chosen from two neighboring delay cells to generate a new phase, where two signals intersect. However, it

requires extra comparators which need more area and more power.

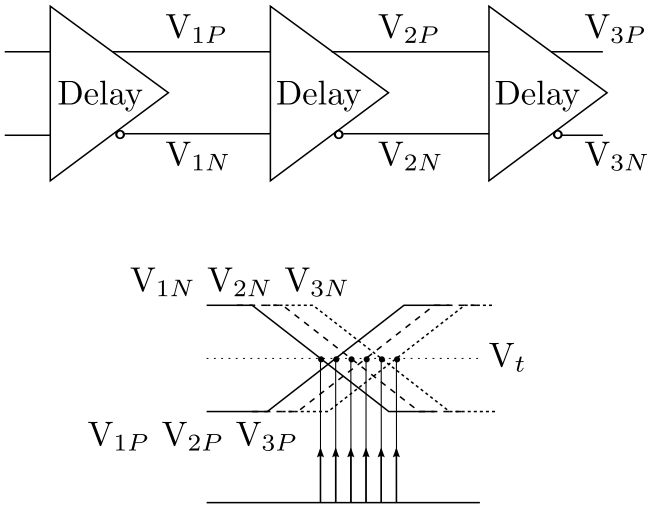

Figure 4.5: Proposed phase interpolation scheme

In this work, we use the phase interpolation scheme, shown in Figure 4.5. Both positive and negative outputs of delay cells are used to generate phases. Two phases are generated at the locations where positive and negative signals intersect with the threshold voltage of latches, V_t. No comparators are required. Note that the positive and negative outputs need to change at different times. Figure 4.6 shows the multiple-pass delay cell used in this work, where $P+$ and $P-$ are primary inputs, and $S+$ and $S-$ are the secondary inputs which receive earlier trigger signals. At the beginning of the operation, $S+$ and $S-$ change from low to high and from high to low, respectively, while $P+$ and $P-$ stay low and high, respectively. $O+$ starts to change slowly from high to weak high. When $P+$ and $P-$ change from low to high and from high to low, respectively, $O+$ changes to high immediately, while $O-$ becomes weak high. When the high voltage at $O+$ propagates to M_1 via M_3, whose speed is

controlled by V_c, $O-$ changes to low. Then $O+$ and $O-$ are connected to $P-$ and $P+$ of the next delay cell, respectively. In this structure, an extra phase can be generated, since $O+$ and $O-$ change at different times.

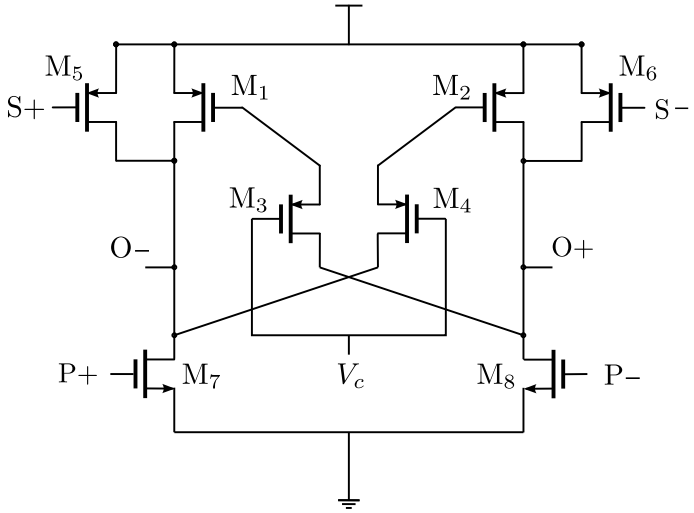

Figure 4.6: The multiple-pass delay cell.

4.4 Simulation results

The proposed multiple-pass delay-line ADC is designed and simulated in a commercial 40 nm CMOS process. Table 4.1 shows the summary of the simulation results. The high frequency simulation is done by applying a 173 MHz sinusoidal input. In order to increase resolution, the phase interpolation technique, described in Section 4.3, is used. Figure 4.7(a) illustrates the spectrum of the simulation result with the phase interpolation technique, while Figure 4.7(b) shows the spectrum without phase interpolation. With phase interpolation, SNDR is improved by 4.3 dB. The signal-to-noise-plus-distortion

Technology	40nm CMOS
Supply Voltage	1.1V
Sampling Rate	500MS/s
Number of Bits	7
Differential input range	0.8V p-p
SNDR @ 173 MHz	37.0dB
SFDR @ 173 MHz	45.0dB
Power Consumption	4.2mW

Table 4.1: Performance summary of the multiple-pass delay-line ADC.

ratio (SNDR) and the spurious free dynamic range (SFDR) are 37.0 dB and 45.0 dB, respectively, which provide an effective number of bits (ENOB) = 5.86 bits.

To compare the multiple-pass delay line ADC to other work in terms of power consumption, sampling rate, and resolution, the figure of merit (FOM) is used [42].

$$\text{FOM} = \frac{Power}{2^{\text{ENOB}} \times \min(2f_{\text{in}}, f_{\text{sample}})}$$

The FOM of the proposed multiple-pass delay-line ADC is 0.145 pJ/conversion-step at 500MS/s and a 1.1 V supply. Table 4.2 shows the comparison between the proposed multiple-pass delay-line ADC and other state-of-the-art ADCs. It shows that the multiple-pass delay-line ADC can achieve a competitive FOM with other reported ADCs.

Reference	Architecture	Technology	f_s (GS/s)	# of Bits	Power (mW)	Calibration	FOM (pJ/Conv.-step)
[32]	Flash	180nm	4	4	78	Foreground	4.3
[41]	Folding-Flash	65nm	1.75	5	2.2	Foreground	0.05
[46]	SAR	65nm	1	6	6.7	Foreground	0.21
[28]	Folding-Flash	90nm	2.7	6	50	Background	0.47
[4]	SAR	130nm	1.25	6	32	Background	0.785
[14]	SAR	65nm	0.25	5	1.2	Redundancy	0.24
[36]	Flash	90nm	2	4	10	None	19.4
[17]	Flash	130nm	1.6	6	180	None	2.6
[6]	Two-step Flash	130nm	1	6	49	None	1.24
[40]	Delay-Line	65nm	1.2	5	2	None	0.196
This work	Delay-Line	40nm	0.5	7	4.2	None	0.145

Table 4.2: Performance comparison of state-of-the-art work.

4.5 Conclusion

In this work, we proposed a 7-bit multiple-pass delay-line ADC. In our simulation results, the SNDR and SFDR are 37.0 dB and 45.0 dB. In order to increase phases, phase interpolation technique is used. The SNDR is improved from 34.2 to 37.0 dB after applying phase interpolation. No calibration technique is used. As a result, the multiple-pass delay-line ADC with the phase interpolation technique can resolve the linearity issue of delay-line ADCs.

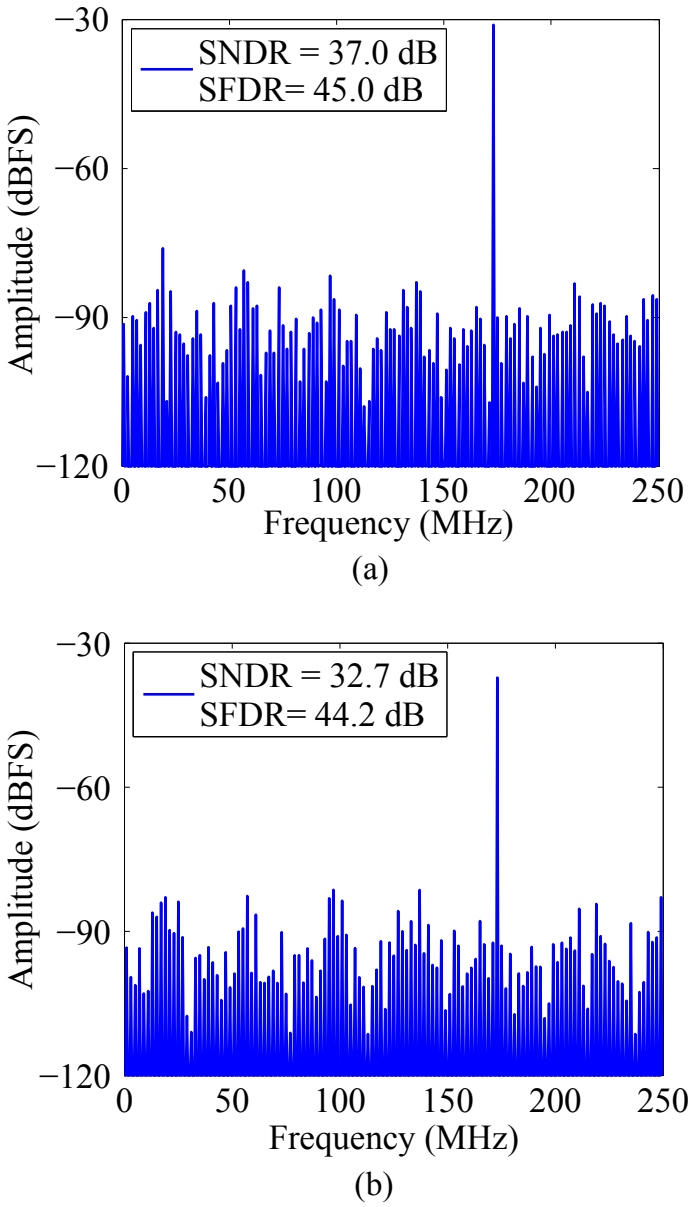

Figure 4.7: Output spectrum of a 173 MHz sinusoid input. (a) With phase interpolation (b) Without phase interpolation.

Chapter 5

Conclusions

In this dissertation, we introduced a novel architecture, digital calibration techniques, and a multiple-pass delay line ADC to improve the linearity of delay-line ADCs, since delay-line ADCs are becoming more and more attractive when process dimensions shrink to nano scales. These architectures and techniques significantly lessen the impact of the non-linearity of delay-line ADCs on the overall ADC performance.

First of all, the proposed hybrid ADC, a 4-bit flash ADC followed by a 7-bit delay-line ADC, significantly reduces the noise of the second-stage delay line ADC in the output of the hybrid ADC. The achieved FOM, 33.8 fj/conv-step, is competitive with that of state-of-the-art ADCs.

Secondly, in order to remove the harmonic distortion of delay-line ADCs, we extend HDC to digitally calibrate a delay-line ADC. The simulation results shows thtat the SNDR is improved from 25.6 dB to 42.5 dB after averaging 2^{27} sample points which corresponds to an 860 milliseconds calibration time.

Last, a multiple-pass delay line ADC with a phase interpolation technique is proposed to improve the overall ADC performance in terms of speed and resolution.

Chapter 6

Future Work

6.1 Performance improvement for the Hybrid ADC

In Chapter 2, we presented a Hybrid ADC, where a 4 bit flash ADC is followed by a 7 bit delay-line ADC. Simulation results show the power of the pre-amplifiers dominates the overall power consumption. The tail current of the pre-amplifiers is biased at 47 μA. Thus, a power-saving technique is adopted by setting the bias voltage to 250 mV, which can reduce the tail current to 5 μA. However, this method also increases the complexity of the design.

In order to simplify the design and further reduce the overall power consumption, several possible future research directions should be considered. First, a dynamic comparator with a current source [20], shown in Figure 6.1, is used instead of a regenerative latch. The dynamic comparator with a current source has been proven successfully to derive a 10-bit resolution [25]. Thus, we believe that using the dynamic comparator with a current source to replace the regenerative latch can significantly reduce total power, since the pre-amplifiers in the first-stage flash ADC are no longer needed.

Another direction is a two-stage delay-line ADC, where a 4-bit delay line is substituted for the original 4-bit flash ADC. Figure 6.2 shows the diagram of the two-stage delay-line ADC, where a 4-bit delay line ADC is

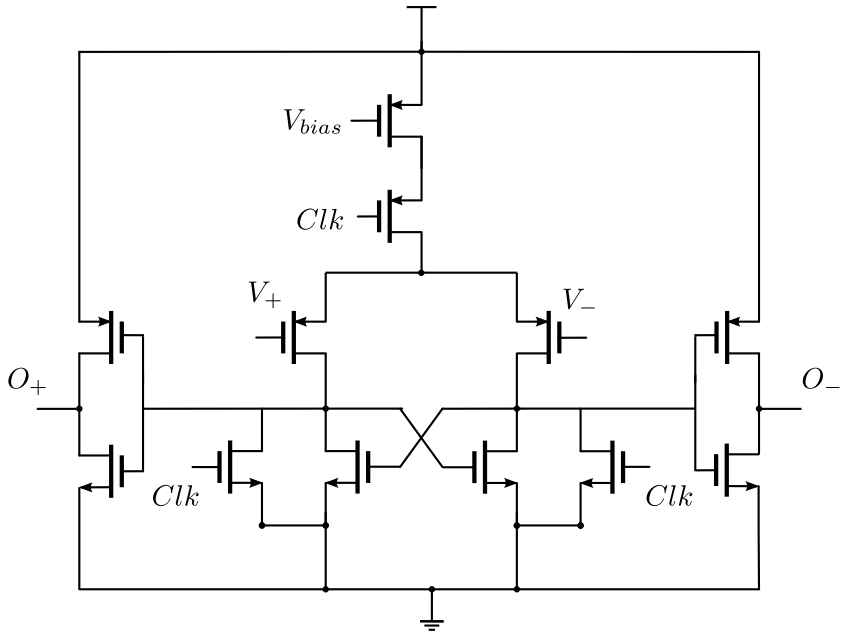

Figure 6.1: Dynamic comparator with a current source.

followed by a 7-bit delay-line ADC. Although the 4-bit delay introduces error/distortion, the 4-bit DAC can provide an accurate result to the second stage, and then the second-stage ADC generate a finer result, which can correct the error/distortion generated in the first-stage delay-line ADC. Also, in [13], the authors show that the noise of the sub-DAC limits the performance of pipelined ADCs. Therefore, we expect that the two-stage delay-line ADC can also greatly improve the overall power consumption without sacrificing resolution.

6.2 Convergence time reduction for digital calibration

In Chapter 3, we extended the harmonic distortion correction technique for the calibration of a delay line ADC. In simulation results, after enabling

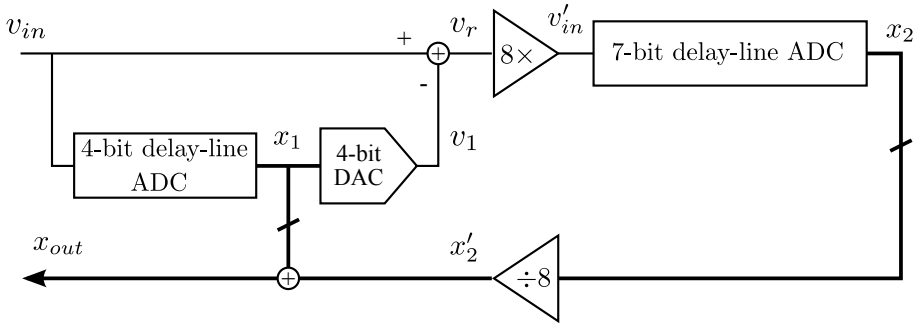

Figure 6.2: The two-stage delay-line ADC architecture.

the harmonic distortion correction technique, the SNDR is significantly improved to 42.5 dB by averaging 2^{27} points, which corresponds to a 0.86 second calibration time. However, the convergence time is still a concern. A longer calibration time implies larger power consumption and a longer start-up time. Therefore, the improvement of the convergence time should be studied in the future.

Bibliography

[1] A. Abidi *et al.*, "Phase noise and jitter in cmos ring oscillators," *Solid-State Circuits, IEEE Journal of*, vol. 41, no. 8, pp. 1803–1816, 2006.

[2] A. M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," *Solid-State Circuits, IEEE Journal of*, vol. 34, no. 5, pp. 599–606, 1999.

[3] M. Boulemnakher, E. Andre, J. Roux, and F. Paillardet, "A 1.2 V 4.5 mW 10b 100MS/s pipeline ADC in a 65nm CMOS," *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, pp. 250–611, 2008.

[4] Z. Cao, S. Yan, and Y. Li, "A 32 mW 1.25 GS/s 6 bit 2 b/Step SAR ADC in 0.13 μm CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 3, pp. 862–873, 2009.

[5] Y. Chai and J.-T. Wu, "A 5.37 mW 10b 200MS/s dual-path pipelined ADC," *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, pp. 462–464, 2012.

[6] H.-W. Chen, I.-C. Chen, H.-C. Tseng, and H.-S. Chen, "A 1-GS/s 6-Bit two-channel two-step ADC in 0.13-m CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 11, pp. 3051–3059, 2009.

[7] Y. Chiu, B. Nikoli, and P. Gray, "Scaling of analog-to-digital converters into ultra-deep-submicron cmos," *Custom Integrated Circuits Conference,*

2005. Proceedings of the IEEE 2005, pp. 375–382, 2005.

[8] Y. Chiu, "High-performance pipeline A/D converter design in deep-submicron CMOS," Ph.D. dissertation, University of California, Berkeley, 2004.

[9] Y. Chiu, C. W. Tsang, B. Nikolic, and P. R. Gray, "Least mean square adaptive digital background calibration of pipelined analog-to-digital converters," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 51, no. 1, pp. 38–46, 2004.

[10] J. Chu, L. Brooks, and H.-S. Lee, "A zero-crossing based 12b 100MS/s pipelined ADC with decision boundary gap estimation calibration," *VLSI Circuits (VLSIC), 2010 IEEE Symposium on*, pp. 237–238, 2010.

[11] D. W. Cline and P. R. Gray, "A power optimized 13-b 5 Msamples/s pipelined analog-to-digital converter in 1.2 μm CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 31, no. 3, pp. 294–303, 1996.

[12] Y. A. Eken and J. Uyemura, "A 5.9-GHz voltage-controlled ring oscillator in 0.18-μm cmos," *Solid-State Circuits, IEEE Journal of*, vol. 39, no. 1, pp. 230–233, 2004.

[13] I. Galton, "Digital cancellation of D/A converter noise in pipelined A/D converters," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 47, no. 3, pp. 185–196, 2000.

[14] B. P. Ginsburg and A. P. Chandrakasan, "Highly interleaved 5-bit, 250-MSample/s, 1.2-mW ADC with redundant channels in 65-nm CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 12, pp. 2641–2650, 2008.

[15] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and phase noise in ring oscillators," *Solid-State Circuits, IEEE Journal of*, vol. 34, no. 6, pp. 790–804, 1999.

[16] S. Henzler, S. Koeppe, D. Lorenz, W. Kamp, R. Kuenemund, and D. Schmitt-Landsiedel, "A local passive time interpolation concept for variation-tolerant high-resolution time-to-digital conversion," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 7, pp. 1666–1676, 2008.

[17] A. Ismail and M. Elmasry, "A 6-bit 1.6-GS/s low-power wideband flash ADC converter in 0.13-m CMOS technology," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 9, pp. 1982–1990, 2008.

[18] T.-K. Jang, J. Kim, Y.-G. Yoon, and S. Cho, "A highly-digital VCO-based analog-to-digital converter using phase interpolator and digital calibration," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 20, no. 8, pp. 1368–1372, 2012.

[19] D.-Y. Jeong, S.-H. Chai, W.-C. Song, and G.-H. Cho, "Cmos current-controlled oscillators using multiple-feedback-loop ring architectures," *Solid-State Circuits Conference, 1997. Digest of Technical Papers. 43rd ISSCC., 1997 IEEE International*, pp. 386–387, 1997.

[20] S. Jiang, M. A. Do, K. S. Yeo, and W. M. Lim, "An 8-bit 200-MSample/s pipelined ADC with mixed-mode front-end S/H circuit," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 55, no. 6, pp. 1430–1440, 2008.

[21] H.-C. Lee and J. A. Abraham, "Digital Calibration for 8-bit Delay Line ADC Using Harmonic Distortion Correction," *Test Symposium (ATS),*

2013 22nd Asian, pp. 128–133, 2013.

[22] ——, "A novel low power 11-bit hybrid ADC using flash and delay line architectures," *Design, Automation and Test in Europe Conference and Exhibition (DATE), 2014*, pp. 1–4, 2014.

[23] S.-J. Lee, B. Kim, and K. Lee, "A novel high-speed ring oscillator for multiphase clock generation using negative skewed delay scheme," *Solid-State Circuits, IEEE Journal of*, vol. 32, no. 2, pp. 289–291, 1997.

[24] G. Li, Y. Tousi, A. Hassibi, and E. Afshari, "Delay-line-based analog-to-digital converters," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 56, no. 6, pp. 464–468, 2009.

[25] C.-C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," *Solid-State Circuits, IEEE Journal of*, vol. 45, no. 4, pp. 731–740, 2010.

[26] C.-C. Liu, S.-J. Chang, G.-Y. Huang, Y.-Z. Lin, C.-M. Huang, C.-H. Huang, L. Bu, and C.-C. Tsai, "A 10b 100MS/s 1.13 mW SAR ADC with binary-scaled error compensation," *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International*, pp. 386–387, 2010.

[27] A. Mesgarani, H. Fu, M. Yan, A. Tekin, H. Yu, and S. Ay, "A 5-bit 1.25 GS/s 4.7 mW delay-based pipelined ADC in 65nm CMOS," *Circuits and Systems (ISCAS), 2013 IEEE International Symposium on*, pp. 2018–2021, 2013.

[28] Y. Nakajima, A. Sakaguchi, T. Ohkido, N. Kato, T. Matsumoto, and M. Yotsuyanagi, "A background self-calibrated 6b 2.7 GS/s ADC with

cascade-calibrated folding-interpolating architecture," *Solid-State Circuits, IEEE Journal of*, vol. 45, no. 4, pp. 707–718, 2010.

[29] A. Panigada and I. Galton, "Digital background correction of harmonic distortion in pipelined ADCs," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 53, no. 9, pp. 1885–1895, 2006.

[30] ——, "A 130 mW 100 MS/s pipelined ADC with 69 dB SNDR enabled by digital harmonic distortion correction," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 12, pp. 3314–3328, 2009.

[31] C.-H. Park and B. Kim, "A low-noise, 900-mhz vco in 0.6-μm cmos," *Solid-State Circuits, IEEE Journal of*, vol. 34, no. 5, pp. 586–591, 1999.

[32] S. Park, Y. Palaskas, and M. P. Flynn, "A 4-GS/s 4-bit flash ADC in 0.18-μm CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 9, pp. 1865–1872, 2007.

[33] J. Rabaey, A. Chandrakasan, and B. Nikolić, *Digital Integrated Circuits, 2/E*. Prentice Hall, 2003.

[34] A. Sanyal, K. Ragab, L. Chen, T. Viswanathan, S. Yan, and N. Sun, "A hybrid SAR-VCO $\Delta\Sigma$ ADC with first-order noise shaping," *Custom Integrated Circuits Conference (CICC), 2014 IEEE Proceedings of the*, pp. 1–4, 2014.

[35] E. Siragusa and I. Galton, "A digitally enhanced 1.8 v 15 b 40 MS/s CMOS pipelined adc," *Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International*, pp. 452–538, 2004.

[36] D. A. Sobel and R. W. Brodersen, "A 1 Gb/s mixed-signal baseband analog front-end for a 60 GHz wireless receiver," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 4, pp. 1281–1289, 2009.

[37] H. Song and D.-K. Jeong, "Analysis and design of fast settling voltage-controlled delay line with dual-input interpolating delay cells," *Electronics letters*, vol. 46, no. 11, pp. 749–750, 2010.

[38] Y. Sugimoto and T. Ueno, "The design of a 1 V, 1 GHz CMOS VCO circuit with in-phase and quadrature-phase outputs," *Circuits and Systems, 1997. ISCAS'97., Proceedings of 1997 IEEE International Symposium on*, vol. 1, pp. 269–272, 1997.

[39] L. Sun, T. Kwasniewski, and K. Iniewski, "A quadrature output voltage controlled ring oscillator based on three-stage sub-feedback loops," *Circuits and Systems, 1999. ISCAS'99. Proceedings of the 1999 IEEE International Symposium on*, vol. 2, pp. 176–179, 1999.

[40] Y. Tousi and E. Afshari, "A Miniature 2 mW 4 bit 1.2 GS/s Delay-Line-Based ADC in 65 nm CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 46, no. 10, pp. 2312–2325, 2011.

[41] B. Verbruggen, J. Craninckx, M. Kuijk, P. Wambacq, and G. Van der Plas, "A 2.2 mW 1.75 GS/s 5 bit folding flash ADC in 90 nm digital CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 3, pp. 874–882, 2009.

[42] ——, "A 2.2 mW 5b 1.75 GS/s folding flash ADC in 90nm digital CMOS," *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, pp. 252–611, 2008.

[43] B. Verbruggen, M. Iriguchi, and J. Craninckx, "A 1.7 mW 11b 250MS/s 2× interleaved fully dynamic pipelined SAR ADC in 40nm digital CMOS," *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, pp. 466–468, 2012.

[44] T. Watanabe, T. Mizuno, and Y. Makino, "An all-digital analog-to-digital converter with 12-μv/lsb using moving-average filtering," *Solid-State Circuits, IEEE Journal of*, vol. 38, no. 1, pp. 120–125, 2003.

[45] Wgsimon, "Transistor Count and Moore's Law - 2011," available online at http://commons.wikimedia.org/wiki/User:Wgsimon.

[46] J. Yang, T. L. Naing, and R. W. Brodersen, "A 1 GS/s 6 bit 6.7 mW successive approximation ADC using asynchronous processing," *Solid-State Circuits, IEEE Journal of*, vol. 45, no. 8, pp. 1469–1478, 2010.

[47] M. Yoshioka, K. Ishikawa, T. Takayama, and S. Tsukamoto, "A 10b 50MS/s 820μW SAR ADC with on-chip digital calibration," *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International*, pp. 384–385, 2010.